FINAL REPORT - VOLUME 2

ELECTRICAL CHARACTERIZATION OF THE RCA CPD1822SD RANDOM ACCESS MEMORY

JUNE 1979

(NASA-CR-162260) ELECTRICAL
CHARACTERIZATION OF THE RCA CPD1822SD RANDOM
ACCESS MEMORY, VOLUME 2, Final Report
(Hughes Aircraft Co.) 432 p HC A19/MF A01
CSCL 09B G3/60

N79-31960

Unclas 31899

CONTRACT JPL 954789

AEROSPACE GROUPS

HUGHES

HUGHES AIRCRAFT COMPANY CULVER CITY, CALIFORNIA



JPL Subcontractor Report

JPL FILE NO. 9950- 156

TITLE	ELECTRICAL CHARACTERIZAT	TION OF THE RCA CPD1822SD RANDOM ACCESS MEMORY
AUTHOF	R(S) A. Klute	
SUBCON	NTRACTOR Hughes Airc	raft Company: Aerospace Groups
	NTRACTOR REPORT NO	Final Report, Volume 2 (Appendix B and C) (Hughes Report No. FR-79-76-867)
REPORT	DATE	PERIOD COVERED
JPL COI	NTRACT NO954789, M	Modification 1 PAGE COUNT

8/15/79kw

4 copies: 2-NASA, 2-Vellum

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ELECTRICAL CHARACTERIZATION OF THE RCA CDP1822SD RANDOM ACCESS MEMORY

Volume 2 FINAL REPORT JUNE 1979

(Appendix B and C) Contract Number JPL 954789, Modification 1

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Hughes Aircraft Company • Culver City, California

APPENDIX B

	e de la ballita como como en la despois de despois de la como de la como de la como como como como como como como com		
RCA CDP18228D 256 X 4	CMOS STATIC RAM	31 AUG 78 TEMPI	25 C SN:
		PAGE	1 OF 10
	ITS) VCC=10V		
PASSED GALPAT (TIGHT LIN PASSED GALPAT (TIGHT LIN		REPRODUCIBILITY (ORIGINAL PAGE IS	
PASSED DATA RETENTION TES	3.T	OMORPHIC LINES IN	100K
MODER BRAN MISERIAN IEC	, ,		
	VCC = 4.5V	5.0V	10'.0V
ADDRESS ACCESS TIME	(TAA) 315.N	255 N	95,0N
DATA SETUP TIME	(TDS) 38,0N	30.0N	10,0N
DATA HOLD TIME	(TDH) 10'.0N	10 ON	15,00
ADDRESS SETUP TIME	(TAS1) 18,0N	14.0N	4.00N
ADDRESS SETUP TIME	(TAS2) 144.N	118.N	56,0N
ADDRESS HOLD TIME	NO.85- (HAT)	~25° ₩	-6.00N
WRITE PULSE WINTH	(TWP) 100.N	86.0N	0 4 a 8 N
CS1 SETUP TIME	(TCSS1) 224.N	186'N 182'N	84,0N
CS2 SETUP TIME	(TCSS2) 218.N	182.N	85 ⁵ 8 M
CS1 HOLD TIME	(TESH1) 62,0N	54. ØN	28,0N
CS2 HOLD TIME	(TCSH2) 66.0N	56.AN	28,0N
OUTPUT ACTIVE FROM CS1	(TDOA1) 290.N	242.M	126.N
OUTPUT ACTIVE FROM CS2	(TDOAZ) 286.N	N. BES	104 e N
OUTPUT ACTIVE FROM MRD	(7D0A3) 66.0N	5A. ØN	NS. CF
OUTPUT HOLD FROM CS:	(TDOH1) 166.N	132,N	38, ØN
OUTPUT HOLD FROM CS2	(TOOH2) 160.N	128, N	38,0N
OUTPUT HOLD FROM MRD	(TDAH3) (42.N	128, N 120, N	38,0N
OUTPUT HOLD FROM MWR	(TPOH) 142.N	116 _p N	40.0N
READ CYCLE TIME	(TRC) 320.N	264, N	120 N
WRITE CYCLE TIME	(TWC) 318.N	272.N	136.N

	TIL	IIH	VICI	A1C5
AD A1 A2	-2.60NA -2.60NA -2.40NA	2,40NA 2,79NA 2,30NA	3,50 V 3,52 V 3,54 V	-3/51 V -3/52 V -3/57 V -3/57 V
AB	-2.70NA	2.70NA	3.53 V	-3',57 V
A4 A5 A6 A7	-2,50NA -2,40NA -2,30NA -2,60NA	2.60NA 3.00NA 2.90NA ANOC.5	3,54 V 3,45 V 3,49 V 3,47 V	93,57 V 93,58 V 93,58 V 93,53 V
CS1 CS2 MWR MRD	=2.60NA #2.70NA =2.80NA =2.40NA	2.60NA 2,60NA 2,50NA 2.40NA	3.51 V 3.56 V 3.49 V 3.51 V	-3,55 V -3,56 V -3,50 V
010 110 510 510	-2.30NA -2.40NA -2.70NA -2.50NA	2,30NA 2,40NA 2.80NA 2,40NA	3.61 V 3.61 V 3.60 V 5.59 V	=5,57 V =3,55 V =3,55 V =5,54 V

RCA	CDP18228D	256 X 4 CMOS	STATIC RAH	31 AUG 78
	ppø	001	sag	D03
VOL1 VOL2 VOH1	120.MV 120.MV 4.82 V 9.76 V	120', MV 130', MV 4, 62 V 9, 76 V	130 MV 145 MV 4 82 V 9 75 V	125, MV 140, MV 4,82 V 9,76 V
IDN1 IDN1 IDP1 IDP2	AMQC_8 AMT_121 AME1_S=	6.10MA 14.8MA -2.13MA -5.03MA	5-75MA 13-2MA -2-10MA -4-89MA	5,85MA 13,6MA 22,13MA 45,05MA
IOZ1 IOZ2 IOZ3 IOZ4	21.6NA 24.6NA 19.0NA 17.9NA	22,8NA 19,2NA 23,4NA 24.8NA	20,3NA 23,8NA 20,2NA 18.6NA	22,3NA 19,0NA 21.8NA 24,5NA
1025 1026 1027 1028	25,2NA 24,9NA	18,1NA 18,2NA 18,3NA 17.8NA	25,8NA 25,7NA 25,9NA 25,6NA	17,6NA 17,4NA 17,3NA 17,4NA
ILDP	#10,0UA			
IL1 IL2 IL3 IL4	-5.00UA -5.00UA -5.00UA			

PÂGE

2 OF 10

RCA CDP18225D 256 X 4 CMOS STATIC RAM 31 AUG 78 TEMP! -20 C SN:

PASSED GALPAT (WIDE LIMITS) VCC=10V PASSED GALPAT (TIGHT LIMITS) VCC=10V PASSED GALPAT (TIGHT LIMITS) VCC=5V

to the state of th	· · · · · ·			
	vcc	= 4,5V	5 . øv	1,0'. 0V
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA) (TDS) (TDH)	335 N 44 UN 8 NON	260'N 32'0N 8'00%	90.0N 8.00N 10.0N
ADDRESS SETUP TIME ADDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WIDTH	(TAS1) (TAS2) (TAH) (TWP)	30.0N 146.N -26.0N 112.N	20.0N 118.N -20.0N 92.0N	4.00N 50.0N -4.00N 40.0N
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS1) (TCSS2) (TCSH1) (TCSH2)	228.N 222.N 58.0N 58.0N	186, N 182, N 48, ØN 50, ØN	78,0N 76,0N 26,0N 24,0N
OUTPUT ACTIVE FROM CS1 OUTPUT ACTIVE FROM CS2 OUTPUT ACTIVE FROM MRD	(IADOT) (SADOT) (EADOT)	298 N 294 N 62 0	238, N 236, N 52. An	98,42 96,00 28,00
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR DUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH1) (TDOH2) (TDOH3) (TPOH) (TRC) (TWC)	156.N 154,N 140.N 138.N 312.N 320.N	124 N 120 N 118 N 114 N 248 N 256 N	24 6 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8
IIL I	ІН	VICI	VICP	
A1 -300.PA 30 A2 #300.PA 20	00.PA 00.PA 00.PA 00.PA	3.51 V 3.53 V 3.54 V 3.53 V	-3,51 V -3,52 V -3,56 V -3,57 V	
A5 =300,PA 40 A6 =200,PA 40	OD,PA OU,PA OO,PA OO,PA	3.54 V 3.46 V 3.50 V 3.48 V	43,57 V 43,52 V 43,50 V 43,53 V	
CS2 ~400°4V 30	00 PA 00 PA 00 PA 00 PA	3,51 V 3,56 V 3,50 V 3,51 V	93,53 V 93,55 V 93,50 V 93,51 V	
DI1 =200,PA 30 DI2 =300,PA 30	00'.PA 00'.PA 00'.PA	3.61 V 3.61 V 3.50 V 3.59 V	-3,57 v -3,55 v -3,55 v -3,53 v	

RÇA	CDP18225D	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEHPI	-20 C S
					PÄGE	4 OF 10
	BOO	001	saa	003		•
VOL1 VOH1 VOH2	105,MV 105,MV 4,85 V 9,80 V	105, MV 110, MV 4,84 V 9,79 V	115,MV 125,MV 4,84 V 9.79 V	110, MV 120, MV 4,84 V 9,80 V		
IDN1 IDN2 IUP1 IDP2	7.00MA 17.8MA =2.55MA =5.97MA	6.85MA 17.0MA -2.53MA -5.96MA	6.45MA 15.2MA 42.48MA 45.82MA	6 55MA 15.7MA 12,55MA 46.04MA		
10Z1 10Z2 10Z3 10Z4	1.60NA 4.20NA 3.60NA 900.PA	6,80NA 3,50NA 3,50NA 7.20NA	700.PA 3.60NA 4.60NA 1.10NA	7,00NA 4,20NA 2,30NA 5,80NA		
1025 1026 1027 1028	7.40NA	900', PA 1', 00NA 1', 00NA 900', PA	6,20NA 6,40NA 6,40NA	1,40NA 1,40NA 1,40NA 1,30NA		
ILDP	#5.00UA					
173 173 175	#5,00UA #5,00UA #5,00UA					

SN:

RCA CDP1822SD 256 X 4 CMOS STATIC RAM 31 AUG 78 TEMPI -55 C SN:

PAGE 5 OF 10

PASSED	GALPAT	(海IDE	LIMITS	ACC≍IQA	
			LIMITS)	VCC≖10V VCC≖5V	REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

	VCC	= 4,5V	5 ' ,0V	10.0V
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA) (TDS) (TDH)	330 • N 58 • 00 8 • 00N	250'.N 40'.ON 8'.DON	85,0N 10.0N 8.00N
ADDRESS SETUP TIME ADDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WINTH	(TAS1) (SEAT) (HAT) (GWT)	34'0N 144'N -26'0N 104'N	18.0N 114.N -20.0N 94.0N	4.00k 46.0k -0.70k -0.0k
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS1) (TCSS2) (TCSH1) (TCSH2)	232.N 232.N 74.0N 76.0N	174, N 182. N 60. ON 62. ON	76, dn 70, dn 24, dn 24, Jn
OUTPUT ACTIVE FROM CS OUTPUT ACTIVE FROM CS OUTPUT ACTIVE FROM MR	(SAUDT) S	298 N 296 N 58 DN	232, n 230, n 50, 0n	ଜନ୍ମ ଅନ ଜନ୍ମ ଅନ ଜନ୍ମ ଅନ
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM CS2 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH1) (TDOH2) (TDOH3) (TPOH) (TRC)	152.n 148.n 138.n 138.n 138.n 288.n	116°N 114°N 116°N 112°N 212°N 272°N	100 mm m
IIL	IIH	AZC 8	VTCZ	
A1 -100.PA A2 0.00 A	100 PA 100 PA 100 PA 100 PA	3.54 V 3.56 V 3.56 V	=3,50 V =3,59 V =3,60 V	
A5 -100.PA A6 +100.PA	100,PA 100,PA 100,PA 100.PA	5,57 V 5,49 V 5,53 V 5,50 V	93,61 V 93,55 V 93,53 V 93,56 V	
CS2 =100.PA MWR =100.PA	100,PA 100,PA 100,FA 100,PA	3,54 V 3,60 V 3,53 V 3,55 V	-3,54 V -3,54 V -3,54 V	
DI1 =100.PA DI2 =100.PA	0.00 A 100,PA 100,PA 100.PA	3.63 V 3.63 V 3.63 V 3.62 V	-3,58 V -3,58 V -3,57 V -3,54 V	

RCA	CDF182250	256 X 4 CMDS	STATIC RAM	31 AUG 78
• • • • • • • • • • • • • • • • • • •				
; ; ;	Dog	001	200	003
VOL1 VOH2 VOH2	100.MV 95.0MV 4.87 V 9.82 V	100, MV 100, MV 4,87 V 9,82 V	105.MV 110.MV 4,87 V 9.82 V	105, MV 110, MV 4, 87 V 9, 82 V
IDN1 IDN2 IDP1 IDP2	7.60MA 19.7MA -2.93MA +6.89MA	7,45MA 18,8MA -2,92MA -6,96MA	7.95MA 17.0MA -2.91MA -6.80MA	7.15MA 17.4MA 22,94MA 46.99MA
1021 1022 1023 1024	#1.00NA 1.10NA 3.30NA =100.PA	5,70NA 3,00NA -700,PA 3,00NA	=1.60NA =600.PA 3.50NA 200.PA	7,40NA 5,70NA 1,20NA 4.60NA
1025 1026 1027 1028	3.10NA 3.30NA 2.80NA 2.90NA	600.PA 700.PA 800.PA 1.10NA	2.10NA 1.60NA 1.80NA 1.30NA	4,10NA 4,10NA 4,50NA 4,70NA
ILDP	-1.20UA			
IL1 IL2 IL3 IL4	≃5,00UA =5,00UA ⇒5,00UA ⇒5,00UA			

ī

SN:

TEMP:

PAGE

⇒35 C

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RCA	CDP1822SD	256 X 4	CMOS STATIC	RAM 3	1 AUG 7	8 TEMPI	85 C	SN1
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									PAGE	7	OF	10
PASSED PASSED PASSED	GALPAT	(WIDE (TIGHT (TIGHT	LIMIT	S)	VCC = 1 VCC = 1 VCC = 5	ØV		REPROD ORIGINA	UCIBILITY AL PAGE I	OF T 3 POC	HE R	
PASSED	DATA RET	ENTION	TEST									
				V	CC ≄	4.5	A	5,0	v	10	.øv	ı
DATA SE	ACCESS TUP TIME		(ፕ	AA) DS) DH)		300 40, 12.	ØN	250 32. 12.	, an	10	0.N .ØN)
ADDRESS ADDRESS	S SETUP T S SETUP T S HOLD TI PULSE WID	IME ME	(T (T	AS1) AS2) AH) WP)	**	10, 144 26, 110	.N	8.0 126 -22.	ร ู้ N , ศพ	64 ≖8.	00N 00N 00N	!
CS2 SE	ETUP TIME ETUP TIME DLD TIME	E	(Τ (Τ	CSS1 CSS2 CSH1 CSH2))	232 226 70,	_N	198 194 62.	, DN	92 34	, 0 N p 0 N p 0 N	i
OUTPUT	ACTIVE F ACTIVE F ACTIVE F	ROM CS	2 (7	1A00 SA00 EA00	3	292 288 70.	, N	258 248 62.	3 . N	9 1	A.S. M.S. M.D.	ı
OUTPUT OUTPUT OUTPUT READ CY	HOLD FRO HOLD FRO HOLD FRO CLE TIME YCLE TIME	M CS2 M MRD M MWR	ፕ) ፕ) ፕ) ፕ)	DOH1 DOH2 DOH3 POH) RC) WC))	170 164 144 144 328 260	N N N	128 128	I N R N R N R N R N	60 80 80 81	18.4666 19.0000 19.00000 19.000000 19.0000000 19.0000000000	i I f
	TIL		IIH		V 1	Ci		AICS				
00 A1 A2 A3	#42,9NA #42,7NA #42,0NA #43.3NA		42.8NA 43.0NA 41.8NA 43.4NA		3, 3,	53 55 58	V V	3,54 3,55 3,61 3,61	V			
A4 A5 A6 A7	-40.9NA -42.4NA -41.1NA -42.9NA	4	41.8NA 44.2NA 43.4NA 42.9NA		3, 3.	57 48 52 51	V V	*3,61 *3,54 *3,52 *3,56	V V V			
CS1 CS2 MWR MRD	=42,1NA =41,5NA =42,5NA =41.2NA		41,8NA 43,4NA 41.3NA 41.0NA		3, 3,	54 59 54	V V	#3,57 #3,59 #3,53 #3.54	V V V			
010 011 012 013	#40.5NA #40.7NA #40.9NA #41.0NA		41.4NA 41.6NA 42.1NA 41.5NA		3. 3.	63 64 63 62	V V		V V V			
						-						

RCA	CDP1822SD	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP :	85 C S
					PAGE	8 OF 10
	מטמ	001	500	003		
VOL 1	135.MV	140°, MV	150. MV	150 MV		
AOL'S	145 MY	155.MV	170 MV	165.MV		
VOH1	4.78 V	4,78 V	4,78 V	4 78 V		
AOHS	9.70 V	4,78 V 9,70 V	9.69 V	165 MV 4,78 V 9,71 V		
IDNI	5.45MA	5'.30MA	4.95MA	5,05MA		
IDNS	13.3MA	12.5MA	11,5MA	11.5MA		
IDP:	-1.80MA	-1,80MA	-1, <u>7</u> 8MA	MIB.14		
IDP2	#4.22MA	-4.26MA	#4 13MA	#4.27MA		
7071	164 NA	177, NA	162.NA	168 NA		
1025	161.NA	171,NA	168.NA	162,NA		
1023	158.NA	173,NA	164 NA	162, NA 163, NA		
1024	162,NA	166.NA	171 NA	161.NA		
1025	161.NA	172,NA	179.NA	164, NA		
IOZ6	174.NA	163,NA	167 NA	170 NA		
IOZ7	161.NA	176, NA	161.NA	169, NA		
IOZ8	164.NA	165.NA	173.NA	164.NA		
ILDP	5,00UA					
7L1	≈25,0UA					
175	≈30,0U A					
11.3	∞25,0UA					
IL4	#50_0NV					

SN:

PAGE 9 0F 10

PASSED	GALPAT	(WIDE	LIMITS)	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS)	VCC#5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

	•			
	vcc	8 4.5V	5 . 0v	10'.0V
ADDRESS ACCESS TIME	(TAA)	310.N	265.N	120.N
DATA SETUP TIME DATA HOLD TIME	(TDS) (TUH)	38,0N 14,0N	32.0n 14.0n	12,0N 14.0N
ADDRESS SETUP TIME	(TAS1)	6.00N	5 ่ คลุท	4.90N
ADDRESS SETUP TIME ADDRESS HOLD TIME	(TAS2) (Tah)	752.N N0,85-	_136.N -24.¢N	72,0N 010,0N
WRITE PULSE WINTH	(TWP)	114.H	100.N	54. DN
CS4 SETUP TIME	(TCSS1)	236 . N	204, N	102.N
CS2 SETUP TIME CS1 HOLD TIME	(TCSS2)	239.N	198 N	190.N
CS1 HOLD TIME CS2 HOLD TIME	(TCSH1) (TCSH2)	74° 0N	64.0N	36,0N
·		78.0N	68.0N	36.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	310.N	268, N	134 aN
OUTPUT ACTIVE FROM CS2	(SACOT)	304.N	264 N	130°N
OUTPUT ACTIVE FROM MRD	(TDOA3)	74.0N	66.AN	36.GN
OUTPUT HOLD FROM CS1	(700H1)	170.N	140 N	50,0N
OUTPUT HOLD FROM CS2	(700H2)	166 a N	\$ 36 N	90,8N
OUTPUT HOLD FROM MRD	(TDOH3)	142 N	122, N 122, N	44,9N
OUTPUT HOLD FROM MWR READ CYCLE TIME	(የPDH)	146 N	122 N	46.0N
WRITE CYCLE TIME	(TRC) (TWC)	328 N	280 N	144.5
Milete Fire itule	(1116)	₽ 96 ₀ N	364.3	198.3
TIL JIH	1	VICI	ALCS	
AD ~252.NA 248	NA	3.59 V	.3°,60 V	
	, NA	3.62 V	-3,61 V	
	PNA	3.63 V	=3,66 V	
A3 #248.NA 246	. NA	3.63 V	∞3,66 V	
A4 ~240.NA 238	PNA	3,63 V	-3,66 V	
A5 9248,NA 246	NA	3.53 ∀	93,60 V	
	NΑ	3,58 V	93,58 V 93,63 V	
A7 =250.NA 244	. NA	3.96 V	•3.63 V	
CS1 #245.NA 236	NA	3.60 V	43,63 V	
C82 #238,NA 245	NA	3.64 V	«3,65 V •3,59 V	
MWR =242.NA 237 MRD =239.NA 234		3,56 V	95,59 V	
TING TEST 184 254	. NA	3.59 V	•3.60 V	
PES AN.8ES 010	n N A	3.69 V	•3,66 V	
DI1 -236 NA 241	PNA	3.70 V	-3,63 V	
DIA -234,NA 237		3.69 V	•3,63 V •3,65 V	
013 ~236.NA 236	NA	3,60 V	-3.63 V	

RCA	CDP1822SD	256 X 4 CMD\$	STATIC RAM	31 AUG 78	TEMP	125 C S
					PÄGE	10 OF 10
	DOØ	001	DOZ	003		
VOL 1 VOL 2 VOH 1 VOH 2	150.MV 160.MV 4.76 V 9.67 V	155.MV 170.MV 4.76 V 9.67 V	170.MV 195.MV 4.75 V 9.65 V	165, MV 185, MV 4,76 V 9,67 V		
ION1 ION2 IOP1 IOP2	4.90MA 11.8MA =1.64MA =3.80MA	4'.80MA 11.2MA 41.62MA -3.80MA	4,45MA 9,95MA =1,61MA =3,70MA	4,55MA 17,3MA 21,65MA 3,86MA		
1021 1022 1023 1024	531.NA	553,NA 552,NA 546,NA 552.NA	548.NA 537.NA 539.NA 533.NA	530,NA 535,NA 531,NA 54,NA		
1025 1026 1027 1028	535.NA 521.NA 526.NA 526.NA	553.NA 560.NA 545.NA 552.NA	544 NA 536 NA 543 NA 534 NA	543, NA 530, NA 528, NA 537, NA		

SNI

1LDP	50,0UA
IL1	#125.UA
175	₩150.UA
IL3	110 UA
IL4	- 95.0U∧

RCA	CDP18228D 256	X 4 CMOS ST	ATIC RAM	31 AUG 78	TEMPI	às c
					PAGE	i OF 10
PASSE PASSE PASSE	D GALPAT CTIGH	V EETIMIJ TI	/CC=10V /CC=1V /CC=5V			
PASSE	D DATA RETENTION	N TEST				
		VC	C = 4.5V	5.0V		10.0V
DATA	SS ACCESS TIME SETUP TIME HOLD TIME	(TAA) (TDS) (TDH)	205.N 22.0N 10.0N	175. 18.0 10.0	N	50'.0H 8.70N 12.0N
ADDRE ADDRE	SS SETUP TIME SS SETUP TIME SS HOLD TIME PULSE WIDTH	(TAS1) (TAS2) (TAH) (TWP)	12'.0N 10p.N -16'.0N 68'.0N	10.0 88.0 -12.0 60.0	N N	4.70n 44.0n -4.70n 36.0n
CS1	SETUP TIME SETUP TIME HOLD TIME HOLD TIME	(TCSS1) (TCSS2) (TCSH1) (TCSH2)	146.N 42,0N	130°, 126°, 38°,0 38°,0	N	55°0n 54°0n 64°0n 68°0n
OUTPU	IT ACTIVE PROM (IT ACTIVE FROM (IT ACTIVE FROM)	SE (TOGAE)	194 N	172; 168; 40.0	N	30,0H 30,0H 30,0H
OUTPU OUTPU OUTPU READ	IT HOLD FROM MRC	(TDOH2) (TDOH3)	126.N	9A.8 96.8 108, 104, 192, 176.	N N N N	22°00 24°00 24°00 26°00 26°00 32°00 30°00
	IIL	IIH	VIC1	AACS		
0A 1 1 2 2 3 2 4	91,40NA 91,50NA 91,80NA 91,30NA	1,60na 1,30na 1,20na 2,30na	2.89 V 2.89 V 2.89 V	92,81 V 92,87 V 92,93 V 92,92 V		
A4 A5 A6 A7	#1.40NA #1.50NA #2.00NA #1.40NA	1,30NA 1,70NA 1,40NA 1,40NA	2.88 V 2.82 V 2.85 V	92,91 V 92,86 V 92,88 V 92,88 V		
CS1 CS2 MWR MRD	*1,40NA *2,00NA *1,40NA *1,30NA	1,20NA 1,30NA 1,40NA 1,70NA	2,84 V 2,85 V 2,83 V 2,84 V	92,83 V 92,89 V 92,85 V 92,84 V		
DI0 DI1 DI2 DI3	~1,60NA ~1,60NA ~1,80NA ~1,60NA	1,60NA 1,40NA 1,60NA 1,40NA	2.91 V 2.91 V 2.93 V 2.91 V	e2,87 v e2,85 v e2,85 v	1	
			וו כו			

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RCA	CDP1822SD	256 X 4 CMOS	STATIC RAM	31 AUG 75	TEMP
	•				PAGE
	DOB	001	soa	003	
VOL1	90'_0MV 100 my 4 86 V	95.0MV 105.MV 4,86 V	100.MV 125.MV 4,86 V	100, MV 120, MV 4,86 V	
SHOA	9,79 V	9.79 V	9.78 V	9.80 V	
IDN1 IDN2 IDP1 IDP2	-2.71MA	7,85MA 17.5MA -2,73MA -5.92MA	7.25MA 15.2MA -2,66MA -5.67MA	7.45MA 15.9MA 2.74MA 46.02MA	
10Z1 10Z2 10Z3 10Z4	27 9NA	26,9NA 30,1NA 25.3NA 23,9NA	30,3NA 27,1NA 31,2NA 32,8NA	25.5NA 28.6NA 25.5NA 28.3NA	
1025 1026 1027 1028	22,6NA 22,4NA	31,5NA 31,8NA 31,8NA 31,5NA	26,7NA 26,8NA 26,5NA 26,4NA	ANA, 18 ANA, 18 ANA, DE ANG, DE	
ILDP	-1.20UA				
IL1 IL2 IL3 IL4	=5.00UA =5.00UA =5.00UA				

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	PAGE	3 OF 10
PASSED GALPAT (WIDE LIMITS) VCC=10V PASSED GALPAT (TIGHT LIMITS) VCC=10V PASSED GALPAT (TIGHT LIMITS) VCC=5V	REPRODUCIBILITY ORIGINAL PAGE IS	OF THE POOR
PASSED DATA RETENTION TEST	• .	
VCC × 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME (TAA) 205.N DATA SETUP TIME (TDS) 22.0N DATA HOLD TIME (TDH) 8.00N	170'N 18.0N 8.00N	70.0N 6.00N 10.0N
ADDRESS SETUP TIME (TAS1) 16,0N ADDRESS SETUP TIME (TAS2) 98,0N ADDRESS HOLD TIME (TAH) -14,0N WRITE PULSE WIDTH (TWP) 70.0N	12,0N .80.0N -12,0N 54.0N	4.00N 38.0N -2.00N 34.0N
CS1 SETUP TIME (TCSS1) 144.N CS2 SETUP TIME (TCSS2) 142.N CS1 HOLD TIME (TCSH1) 38.0N CS2 HOLD TIME (TCSH2) 40.0N	122, N 120, N 34, ON 34, ON	55.0N 55.0N 60.0N 60.0N
OUTPUT ACTIVE FROM CS1 (TDOA1) 192.N OUTPUT ACTIVE FROM CS2 (TDOA2) 190.N OUTPUT ACTIVE FROM MRD (TDOA3) 40.0N	160°, N 158°, N 36° an	84, 0N 82, 0N 82, 0N
OUTPUT HOLD FROM CS1 (TDOH1) 122.N OUTPUT HOLD FROM CS2 (TDOH2) 120.N OUTPUT HOLD FROM MRD (TDOH3) 126.N OUTPUT HOLD FROM MWR (TPDH) 122.N READ CYCLE TIME (TRC) 200.N WRITE CYCLE TIME (TWC) 224.N	92.0N 90.0N 108.N 102.N 176.N	22,000 22,000 20,000 30,000 100,00
IIT IIH AICI	VICA	
A0 =200.PA 200.PA 2.89 V A1 =200.PA 200.PA 2.95 V A2 =300.PA 200.PA 2.97 V A3 =200.PA 500.PA 2.97 V	-3.00 V -3.00 V -2.89 V	
A4	#2,98 V #2,95 V #2,95 V	
CS1 =100.PA 200.PA 2.93 V CS2 =400.PA 200.PA 2.93 V MWR =200.PA 200.PA 2.91 V MRD =100.PA 400.PA 2.93 V	#5"85 V #5"86 V #5"81 V	
DIO =200.PA 300.PA 2,99 V DI1 =300.PA 300.PA 2,99 V DI2 =400.PA 300.PA 3.01 V DI3 =300.PA 200.PA 2.98 V	#2194 V #2193 V #2193 V #2193 V	

RCA	CDP1822SD	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP	-w26 C 3
					PAGE	4 OF 10
	Doø	001	500	003		•
VOL1	75,0MY	80,0MV	90'. ØMV	85. ØMV		
VOLE	85.0MV	95,0MV	105.MV	190 MV	,	
VOHI	4.88 V	4,88 V	4.88 V	4,88 V		
SHOV	9.82 V	9.82 V	9_82 V	4,88 V 9,83 V		
IDN1	9.40MA	9.05MA	8.35MA	8.55MA		
IDNS	55.1MV	20.4MA	17,8MA	18,6HA		
IOP1	-3,23MA	-3,26MA	#3,18MA	#3,29MA		
IDP2	-6.96MA	-7.01MA	-6.76MA	-7.11MA		
IOZ1	ANDE.S	5.60NA	1,40NA	6,40NA		
1072	5.40NA	2,40NA	4,50NA	3,20NA		
IOZ3	S'00NY	4,70NA	3.00NA	3,50NA		•
1024	200.PA	7,50NA	300.PA	ANDS,E ANDS,E ANDS,7		
1025	7.50NA	300', PA	6,90NA	1,20NA		
IOZE	7.30NA	600° PA	7,10NA	1,10NA		
1027	7.50NA	300,PA	6.90NA	1,00NA		
IOZ8	7.30NA	500.PA	7.00NA	1.10NA		

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ILDP	÷5,00UA
ILi	-5,00UA
11.5	-5.00UA
IL3	-5,00UA
IL4	-5.00UA

PAGE 5 OF 10

PASSED	GALPAT	(WIDE	LIMITS)	VCC=10V
PASSED	GALPAT	CTIGHT	LIMITS)	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS)	VCC≖5V

	vcc	= 4.5V	5,0V	10'.0v
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA) (TDS) (TDH)	195.N 26.0N 8.00N	160'.N 20'.an 8'.aan	65,0N 6.00N 10.0N
ADDRESS SETUP TIME ADDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WIDTH	(TAS1) (TAS2) (TAH) (TWP)	14.0N 94.0N -14.0N 70.0N	10.0N 76.0N -12.0N 62.0N	4. 70N 34. CN 42. 70N 32. 6N
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS1) (TCSS2) (TCSH1) (TCSH2)	140.N 136.N 46.0N 48.0N	118,N 114,N 34,0N 38,0N	56'0N 54'0N 28'0N 20'0N
OUTPUT ACTIVE FROM CS1 OUTPUT ACTIVE FROM MRD OUTPUT ACTIVE FROM MRD	(TD0A1) (TD0A2) (EA0UT)	188.N 186.N 38.ØN	152'N 152'N 32'0N	80°6N 78°6N 20°6N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(700H1) (700H2) (700H3) (7PDH) (7RC) (7WC)	114.N 114.N 126.N 122.N 200.N	86.0N 86.0N 106.N 102.N 176.N 168.N	00 200 00 200 00 200 00 200 00 200 00 200
11r II	н	AIG?	vica	
A1 = 100.PA 10 A2 = 100.PA 0.	0.PA 0.PA 00 A 0.PA	7 96 V 2 96 V 2 96 V 4 96 E	02,97 V 03,02 V 03,08 V 03,07 V	
A5 =100,PA 20 A6 =100,PA 10	00 A 0.PA 0.PA 0.PA	3.03 V 2.96 V 2.97 V 3.00 V	63.05 V 93.01 V 93.02 V 93.08 V	
CS2 =100.PA 0.	00 A 00 A 0.PA 0.PA	3.00 V 3.00 V 2.98 V 3.00 V	#57.66 A #32.00 A #32.05 A #32.05 A	
DII =100.PA 10	0°PA 0°PA 0°PA 0°PA	3,06 V 3,06 V 3,08 V 3,06 V	93,00 V 93,00 V 93,00 V 93,00 V	

RCA	CDP1822SD	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP!	#55 C	SNI 2
	٠				PAGE	6 OF 10	7
	noø	001	soo	003		•	
A0H5 A0H7 A0f5 A0F1	70,0MV 75.0MV 4,89 V 9,85 V	75.0MV 80.0MV 4.90 V 9.85 V	80 0MV 95 0MV 4 90 V 9 84 V	75 0MV 90 0MV 4 90 V 9 85 V			
IDN1 IDN2 IDP1 IDP2	-3,69MA	10.0MA .22.9MA -3,78MA -8.11MA	9.35MA 20.2MA -3.71MA -7.82MA	9,55MA 20,9MA 43,81MA 48,16MA		÷	
1021 1022 1023 1024	1.30NA	4,60NA 1,10NA 1,30NA 5,00NA	1.60NA 1.20NA 1.80NA +1.40NA	4,90NA 1,90NA 700,PA 4,40NA			
1025 1026 1027 1028	5.50NA 5.40NA	-1,20NA -1,20NA -1,20NA -1,30NA	4,10NA 4,00NA 4,40NA 4.20NA	₩400, PA ₩400, PA ₩700, PA ₩800, PA			
ILDP	=200.NA						
IL1 IL2 IL3 IL4	~5.00UA ~5.00UA ~5.00UA						

DOA						,	
RCA CDP18225D	256 X	4 CMOS	STATIC R	1E 'MAS	AUG 78	TEMP:	85 C SN:
						PAGE	7 OF 10
PASSED GALPAT	CTIGHT	LIMITS) LIMITS) LIMITS)	VCC=1ØV VCC=1ØV VCC=5V		REPRODU ORIGINAL	ICIBILITY L PAGE IS	OF THE POOR
PASSED DATA RET	ENTION	TEST					
			VCC = 4.	.5v	5.øv		10.0v
ADDRESS ACCESS TO DATA SETUP TIME DATA HOLD TIME	TIME	(TAA) (TDS) (TDH)	21 24 12	0.N .GN	185, 18,0 12,0	i	85.0N 8.90N 14.0N

	VCC	C = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA) (TDS) (TDH)	210.N 24.6N 12.6N	185, N 18, ØN 12, ØN	85.0N 8.00N 14.0N
ADDRESS SETUP TIME ADDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSF WIDTH	(TAS1) (TAS2) (TAH) (TWP)	8.00N 106.N -16,0N 78.0N	8.60N 96.0N -14.0N 70.0N	4. PON 50.0N -4. PON 40.0N
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS1) (TCSS2) (TCSH1) (TCSH2)	156.N 152.N 54.0N 54.0N	136, N 134, N 48, M 48, MN	74,0N 70,0N 30,0N 38,0N
OUTPUT ACTIVE FROM CS1 OUTPUT ACTIVE FROM CS2 OUTPUT ACTIVE FROM MRD	(1AOOT) (SAOOT) (EAOOT)	210.N 206.N 50.0N	186, N 184, N 44, ØN	55.00 60.00 00.00
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH1) (TDOH2) (TDOH3) (TPOH) (TRC) (TWC)	132.N 130.N 130.N 126.N 232.N 216.N	102, N 100, N 110, N 106, N 208, N 192, N	2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2
III. III	1	vici	AICS	
A1 #21.6NA 20. A2 #23,5NA 20.	7NA 6NA 8NA 5NA	2.76 V 2.84 V 2.86 V 2.86 V	#2,77 V #2,84 V #2,89 V #2.89 V	
A5 =21,4NA 21. A6 =23,8NA 21.	3N A 7N A 4N A ØN A	2.85 V 2.77 V 2.78 V 2.82 V	#2'87 V #2'82 V #2'84 V #2'84 V	
CS2 =22,6NA 20. MWR =20,6NA 20.	BNA BNA BNA	2.80 V 2.81 V 2.79 V 2.80 V	=2.79 V =2.85 V =2.81 V =2.80 V	
DIS -21,6NA 20.	9NA 8NA 5NA 9NA	2.88 V 2.88 V 2.90 V 2.88 V	=2,83 V =2,81 V =2,84 V =2,81 V	

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RCA	CDF1822SD	256 X 4 CMOS	STATIC RAM	31 AUG 78 TER	APÍ 85 C SN	i ä
				P	AGE 8 OF 10	
	pgø	001	002	200		
VOL 1	105.MV	110, MV	120 MV	120, HV		
AOT5	120,MV	130.MV	150.HV	145 MV		
VOH1	4,82 V	4,82 V	4,82 V	4,83 V		
AOHS	9,74 V	9.75 V	9,74 V	4,83 V 9,76 V		
IDN1	6.90MA	6.60MA	6.10MA	6 . 30MA	`.	
IDNE	15.9MA	14.6MA	12,7MA	13,3MA		
IDP1	-2.27MA	-2.27MA	-2.21MA	AMELEL AMEE _s e		
IDP2	#4 94MA	-4.97MA	=4,75MA	#5".07MA		
rozi	321.NA	340',NA	364 NA	314, NÁ 319, NÁ		
Ioza	324.NA	335,NA	364,NA	319.NA		
1023	319.NA	336,NA	367.NA	319, NA		
1024	326.NA	335.NA	361.NA	324.NA		
IOZS	325 NA	341,NA	375,NA	334, NA		
IOZ6	329.NA	351,NA	364.NA	336 NA		
IOZ7	320.NA	349,NA	366 NA	323 NA		
IOZ8	331 NA	339.NA	367.NA	328 NA		
:		,	_			
ILDP	-5.00UA					
IL1	≈20,auA					
ILZ	~ 20,0UA					
IL3	-20,0UA					
ΥILΔ	-15 OHA					

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PASSED	GALPAT	(WIDE	LIMITS)	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS	VCC=5V

			_	_
	VCC	= 4.5V	5 . av	10.0V
ADDRESS ACCESS TIME	(TAA)	220.N	195 N	95.ØN
DATA SETUP TIME	(TDS)	24,0N	50°ÚN	8.70N
DATA HOLD TIME	CHQT)	14.0N	14,0N	14.0N
ADDRESS SETUP TIME	(TAS1)	6.00N	6.00N	4 . ØØN
ADDRESS SETUP TIME	(TAS2)	116 N	104.N	58°, 0N
ADDRESS HOLD TIME	(HAH)	-18.0N	=16,0N	≖4.70N
WRITE PULSE WINTH	(TWP)	84 ØN	74 " ØN	44,0N
CS! SETUP TIME	(TCSS1)	166.N	148 N	80, QN
CS2 SETUP TIME	(TCSS2)	1.6.4 ₌ N	144.N	78,0N
CS: HOLD TIME	(TCSH1)	56, ØN	50,0N	32,0N
CS2 HOLD TIME	(TCSH2)	58.0N	52,0N	30.0N
OUTPUT ACTIVE FROM CS	1 (TDOA1)	226 a N	aus, n	126 . N
OUTPUT ACTIVE FROM CS	(SAOOT) S	224.N	គូលឲ្ [*] N	126.N
OUTPUT ACTIVE FROM MR	CEADOT) G	54. ØN	48.0N	30.0N
OUTPUT HOLD FROM CS1	(TDOH1)	142.N	112, N	34, ØN
OUTPUT HOLD FROM CS2	(SHOOT)	140,N	110,N	34,0N
OUTPUT HOLD FROM MRD	(TDOH3)	136.N	116, N	34, ON
OUTPUT HOLD FROM MWR	(TPDH)	134.N	112,N	36, QN
READ CYCLE TIME	(TRC)	248,N	216,N	N_est
WRITE CYCLE TIME	(TWC)	732.N	208.N	SES N
IIL	IIH	VICI	V1C2	
AØ =131,NA	126.NA	2.74 V	-2,75 V	
	124, NA	8°8 A	ශ්දී,81 V	
	123,NA	2,84 V	₹2°88 V	
A3 #127.NA	130.NA	2.84 V	∞2,88 V	
A4 =127,NA	120 NA	2 83 V	-2,86 V	
	123,NA	2.75 V	⊶a'aø v	
A6 #134.NA	124 NA	2.77 V	92,83 V	
A7 -128.NA	155 NA	2.80 V	≈2,83 V	
CS1 -133.NA	117'NA	2'78 V	92,78 V	
CS2 #128.NA	120 ₊ NA	2.79 V	92 ₉ 84 V	
MWR #123.NA	119,NA	2.77 V	₩8°14 Λ	
	155*NY	2.78 V	€2.79 V	
DIØ #124.NA	124.NA	2 86 V	e2,81 V	
DI1 -123,NA	120.NA	2,86 V	92,79 V	
DI2 -124.NA	122,NA	2.89 V	დგ [°] 85 ∧	
AN.SSI** CIO	121.NA	2.86 V	⊲2,79 V	

REA	CDP18228D	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP	125 C S
					PAGE	18 OF 18
	DOØ	D01	pos	D03		•
AOH5 AOH1 AOF3	120.MV 135.MV 4.80 V 9.72 V	125,MV 150,MV 4,80 V 9,72 V	140.MV 170.MV 4.80 V 9.71 V	135,MV 160,MV 4,81 V 9,72 V		
ION1 IOP1 IOP2	6.10MA 14.0MA +2.01MA +4.40MA	5.85MA 13.0MA -2.05MA -4.47MA	5,40MA 11,3MA -2,00MA +4,28MA	5,55MA 11,8MA -2,06MA -4,50MA		
1021 1022 1023 1024	1.52UA 1.50UA 1.50UA 1.50UA	1,57UA 1,58UA 1,57UA 1.58UA	1.66UA 1,65UA 1.66UA 1.65UA	1,47UA 1,48UA 1,48UA 1,48UA		
1025 1026 1027 1028	1.52UA 1.54UA 1.53UA 1.51UA	1,600A 1,600A 1,590A 1,590A	1.71UA 1.69UA 1.68UA 1.67UA	1,50UA 1,50UA 1,50UA 1,50UA		
ILDP	40° 0UA					
IL1 IL2 IL3 IL4	=80',0UA =95,0UA =85,0UA =75,0UA					

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RÇA	COP182280	256	X	4	CMOS	STATIC	RAM	31	AUG	78	TEMP:	25	C	SN:	3

PAGE 1 OF 10

			PAG	C 1 OF 10
PASSED GALPAT (TIGH	T LIMITS) V	CC=10V CC=10V CC=5V	REPRODUCIBILI ORIGINAL PAG	TY OF THE E IS POOR
PASSED DATA RETENTIO	N TEST		Oloroniana a race	-
THEOLO DATA NEIGHTIN	, , , , , , , , , , , , , , , , , ,			
	VC	C = 4,5V	5 , 0v	10',0V
ADDRESS ACCESS TIME	(TAA)	400.N	5 3 0 N	95.0N
DATA SETUP TIME	(TDS)	18,00	16.0N	8 • 0 0 N
DATA HOLD TIME	(HOH)	16.0N	14.0M	15.00
INSPECS SERVES THAT	47.54	m etaili	an the second second	de amounts
ADDRESS SETUP TIME	(TAS1)	8.00N	8,000	4 . 2 ON
ADDRESS SETUP TIME ADDRESS HOLD TIME	(TAS2) (Tah)	142 N	110.N	46,0N
WRITE PULSE WINTH	(TWP)	-18.0N 68.0N	=14,0N 60,0N	-4.00N 36.0N
watte ideac Miniu	Cincy	00 * MM	Ω to [±] to l.t.	3 th = 60 th
CS1 SETUP TIME	(TCSS1)	250 N	140, N	68 ØN
CS2 SETUP TIME	(TCSS2)		136 N	66 ØN
CS1 HOLD TIME	(TCSH1)		36.0N	24,0N
CS2 HOLD TIME	(TCSH2)		38.0N	22,0N
OUTPUT ACTIVE FROM C			286,N	9 0 4 a N
OUTPUT ACTIVE FROM C			585 N	102 N
OUTPUT ACTIVE FROM M	RD (TOOA3)	56 BN	50.0N	76.0N
OUTPUT HOLD FROM CS1	(TOOH1)	154.N	124 N	78,0N 70,8E 70,5E
OUTPUT HOLD FROM CS2		•	120,N	ซล_ตN
OUTPUT HOLD FROM MRD			155 N	ฐ <u>ฮ</u> ู ็ดูN
OUTPUT HOLD FROM MUR		144 N	196, N	ระโดท
READ CYCLE TIME	(TRC)	384.N	288, N	120.N
WRITE CYCLE TIME	(TWC)	200°N	184.N	412.N
IIL	IIH	VIC1	VICE	
2 3. G	4 4 1 7	4 1111	V 1 GF;	
AØ -2.90NA	2.90NA	3.18 V	-3,16 V	
A1 -3.10NA	3,00NA	3.19 V	-3,20 V	
AZ +2,80NA	A NNN E	3.21 V	#3,24 V #3.23 V	
A3 -2.70NA	2.50NA	3.20 V	-3.23 V	
5 /1 T T T (1) /1 1 1	7 000	*** *** ** * * *	7, 20 11	
A4 43,30NA	3,00NA	3.24 V	-3,28 V	
A5 -2,60NA	2,90NA	3,14 V	=3,18 V	
A6 =2,40NA A7 =2,30NA	5.60NA 2.60NA	3,12 V 3,14 V	=3,17 V =3,18 V	
A1 -C.#36NV	E • FLANIA W	Daild A	-mate A	
CS1 -2,80NA	2,60NA	3,23 V	-3,24 V	
CS2 -2,90NA	3,10NA	3 25 V	-3,23 V	
MWR -2.90NA	2,60NA	3.19 V	-3,21 V	
MRD ∞2.70NA	2.80NA	3.22 V	-3.24 V	
PATES TO THE MAINTER	n' ng	And the second second	~gf	
DIØ -2.20NA	2.80NA	3.25 V	-3,21 V	
DI1 -2.40NA	2,60NA	3.25 V	-3,18 V	
DIS #2,60NA	2,50NA	3.30 V	+3,23 V	
DI3 -2,50NA	3.20NA	3.25 V	-3,20 V	
		B-21		

RCA	CDP18228D	256	X	4	CMOS	STAT	īc	RAM	31	AUG	78	
	Dog			001		!	ממ	2		Dt	33	
AOHS AOH1 AOL3 AOL1	115.MV 110.MV 4.86 V 9.79 V		3	1,8 1,8	*MV *MV 6 V 8 V		141 4,1	7 MV 7 MV 84 V 77 V		4	25, M 85, M 86	A Ā
ION1 ION2 IOP1 IOP2	6.75MA 16.8MA -2.67MA -5.85MA		-2	.5. ?,6	SMA SMA SMA BMA	ಪ }	2. 13.	55MA 50MA 58MA 51MA		12,	80M 1.1M 66M 91M	A A
1071 1072 1073 1074	19,4NA 18,9NA 12,7NA 14,9NA		1	4,	6NA 3NA 7NA 3NA	;	21 14	7NA 3NA 1NA 1NA		13	5,9N 5,6N 7,7N 3,8N	Ā Ā
1025 1026 1027 1028	17,4NA 17,4NA 17,6NA 17,4NA		1	4,	8NA 8NA 4NA 6NA	i	19 19 19	4NA 8NA 9NA		13	1.1N 5,9N 5.8N	A
ILDP	⇔10,0UA											
IL1 IL2 IL3 IL4	-35,0UA -65,0UA -10,0UA -40,0UA											

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PASSED	GALPAT	(WIDE	LIMITS)	VCC=10V
PASSED	GALPAT	CTIGHT	LIMITS)	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS	VCC#5V

			•	
	VCC	# 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	49Ø.N	325 N	90', 0N
DATA SETUP TIME	(TDS)	20,0N	16.0N	8.00N
DATA HOLD TIME	(TDH)	12.0N	12.0N	10.0N
Service of the Control of the Contro	(15)		10 2 70	10.00
ADDRESS SETUP TIME	(TAS1)	14.0N	12 ON	4.000
ADDRESS SETUP TIME	(TAS2)	150.N	114.N	40.0N
ADDRESS HOLD TIME	(HAT)	-18,0N	-14.0N	-2.00N
WRITE PULSE WINTH	(TWP)	72.0N	64. NN	34,0N
CS1 SETUP TIME	(TCSS1)	360.N	166 N	64, ON
CS2 SETHP TIME	(TCSS2)	358.N	164 N	<u> </u>
·				62, ØN
CS1 HOLD TIME	(YCSH1)	38,0N	32.AN	82.0N
CS2 HOLD TIME	(TCSH2)	40 . ON	34 . ØN	20.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	434 N	BOE N	98,2N
OUTPUT ACTIVE FROM CS2	(SADOR)	432.N	396.N	96,0៧
OUTPUT ACTIVE FROM MRD	(TDDA3)	52.0N	46.0N	24.04
			·	
OUTPUT HOLD FROM CS:	(TDOH1)	150.N	118 N	36,0H 36,0H
OUTPUT HOLD FROM CS2	(TDOH2)	146.N	114 _p N	3 6 ្Ø∜
OUTPUT HOLD FROM MRD	(TDOH3)	142,N	120°N	୬ 0,0⊍
OUTPUT HOLD FROM MWR	(TPDH)	142.N	114,N	36 ØN
READ CYCLE TIME	(TRC)	400.N	288,N	12.N
WRITE CYCLE TIME	(TWC)	256 N	176.N	104 N
total and extended 1 True	() NG J	C 30 m 4	110211	10461
TIL II	Н	AICI	VICE	
AØ =400.PA 50	Ø _p PA	3.23 V	=3,21 V	
	0 PA	3.24 V	∞3,26 V	
	Ø_PA	3.26 V	-3,29 V	
	0.PA	3.25 V	-3.28 V	
THE STREET OF STREET	D # C P	3.4C.3 9		
	Ø _p PA	3.29 V	-3,3P V	
A5 ⇔400.PA 50	Ø,PA	3.20 V	≘3,23 V	
	0,PA	3.17 V	V ES, E	
	Ø PA	3.19 V	-3.23 V	
CS1 =400.PA 40	Ø,PA	3,29 V	+3,28 V	
-		2 2 2 4 V	-2 43 H	
	Ø,PA	3,30 V	93,27 V	
MWR =500,PA 40	Ø,PA	3,25 V	-3,26 V	
MRD =300,PA 50	0 <u>.</u> P A	3.28 V	~3,29 V	
DIO ~300,PA 50	0.PA	3.30 V	-3,26 V	
	Ø,PA	3.30 V	-3,22 V	
	Ø,PA	3.35 V	+3,28 V	
	Ø.PA	3.30 V	-3.25 V	
man ARABI 12 MEL	w- ep 1 71	-a	~~ +4 B E → Y	

RCA	CDP182250	256 X 4 CMOS	STATIC RAM	31 AÚG 78	TEMPI	+26 C	SN:
					PAGE	4 OF	10
	000	001	200	200			
VOL 1	105.MV	105, MV	115,MV	115, MV	,		
AOH:	95.ØMV 4.88 Y	105.MV	125.MV	115.MV			
VOHE	9,82 V	4,88 V 9,82 V	4,88 V 9,81 V	115'MV 4'88 V 9'82 V			
IDN1	7.00MA	6.80MA	AM25.6	6'.45MÅ			
IDNZ	19.2MA	17.7MA	15 4MA	9 m m m m m m m m m m m m m m m m m m m			
IDPI	-3,12MA	-3,09MA	-3,01MA	16.1MA -3,11MA			•
Ippa	#6,88MA	-6.82MA	#6.55MA	=6.95MA			
1021	5.00NA	3,50NA	5,50NA	2,40NA			
IOZ2	1.60NA	6,50NA	2,26NA	5,7MNA			
IDZ3	6.60NA	2,20NA	5,70NA	3.00NA			
IOZ4	7.20NA	900.PA	7.90NA	700.PA			
1025	800 .PA	8,00NA	800.PA	7',60NA			
1026	700.PA	7,80NA	900.PA	7,70NA			
IOZ7	900.PA	8,00NA	900,PA	7,40NA			
1028	800.PA	7.80NA	1.00NA	7.40NA			

3

ILDP 15.0UA
IL1 -35.0UA
IL2 -60.0UA
IL3 -5.00UA
IL4 +35.0UA

	1-		
RCA CDP1822SD 256 X 4	CMOS STATIC	RAM 31 AUG 78 TEMP	-55 C SN: 3
		PAGE	5 OF 10
PASSED GALPAT (WIDE LIN PASSED GALPAT (TIGHT LIN FAILED GALPAT (TIGHT LIN		V	10 PIN: 004
PASSED DATA RETENTION TES	i T		
	VCC = 4	.5V 5.0V	10.00
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TDS) 2	85.N 355.N 6.0N 20.0N	85,0N 8,00N 10,0N
ADDRESS SETUP TIME ADDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WIDTH	(TAS2) 1 (TAH) -1	0,0N 10.0N 62.N 112.N 8.0N -12.0N 66.0N	36.0N 36.0N 4.0N 32.0N
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS2) 4 (TCSH1) 4	22.N 180.N 22.N 176.N 0.0N 34.0N 8.0N 36.0N	60,00 58,00 22,00 20,00
OUTPUT ACTIVE FROM CS1 OUTPUT ACTIVE FROM CS2 OUTPUT ACTIVE FROM MRD	(SAOGT)	.00K 318,N .00K 318.N 0.0N 42.0N	94.0N 92.0N 22.0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM CS2 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH2) 1 (TDOH3) 1 (TPOH) 1 (TRC) 4	42.N 112,N 38.N 110,N 40.N 118,N .00K 114,N 48.N 320,N 92.N 176.N	34,0N 34,0N 38,0N 38,0N 484.N 48.0N

IIL	ITH	VICI	VICE
#100.PA	100 PA	3.30 V	-3,28 V
			-3,32 V
			#3,35 V
-100 PA	100 PA	3.31 V	-3.35 V
≈200.PA	100 PA	3.35 V	-3,38 V
	100 PA		-3,30 V
			₩3,29 V
-100 PA	100 PA	3.25 V	=3.29 V
-100.PA	100 PA	3.36 V	=3,35 V
			=3,32 V
			-3,32 V
-100.PA	100.PA	3.35 V	=3.36 V
€100,PA	100,PA	3.37 V	-3,32 V
#100.PA			#3.28 V
			-3.34 V
-100.PA	100.PA	3.37 V	-3.30 V
	#100.PA #100.PA #100.PA #100.PA #100.PA #100.PA #100.PA #100.PA #100.PA #100.PA #100.PA	#100.PA 100.PA	#100.PA 100.PA 3.30 V #100.PA 100.PA 3.31 V #100.PA 100.PA 3.31 V #200.PA 100.PA 3.31 V #200.PA 100.PA 3.35 V #100.PA 100.PA 3.25 V #100.PA 100.PA 3.25 V #100.PA 100.PA 3.35 V #100.PA 100.PA 3.35 V #100.PA 100.PA 3.37 V #100.PA 100.PA 3.37 V #100.PA 100.PA 3.35 V #100.PA 100.PA 3.35 V #100.PA 100.PA 3.35 V #100.PA 100.PA 3.35 V

REPRODUCIBILITY OF THE

RCA	CDP1822SD	256 X 4 CMOS	STATIC RAM	31 AUG 78
			•	
	ប្រកួល	DOi	800	003
AOH 3 AOH 1 AOF 5 AOF 1	100.MY 90.0MY 4.89 V 9.85 Y	100.MV 95.0MV 4.89 V 9.84 V	105.MV 110.MV 4.88 V 9.84 V	105'MV 105'MV 4'89 V 9'85 V
IDN1 IDP1 IDP2	7,60MA 21,1MA =3,56MA =7,88MA	7.35MA 19.7MA -3.55MA -7.85MA	6.50MA 17.3MA =3.47MA =7.62MA	7.00MA 17.9MA -3,60MA -8.00MA
1021 1022 1023 1024	3.10NA 5.90NA -1.00NA ~300.PA	1 80NA -1 20NA 5 50NA 4 20NA	1.80NA 5.30NA -1.10NA -1.40NA	2.80NA -600.PA 4.60NA 4.80NA
1025 1026 1027 1028	4.60NA 4.40NA 4.40NA 4.10NA	-1.30NA -1.00NA -1.20NA -800.PA	4.60NA 4.70NA 4.50NA 4.50NA	#1,30NA #1,40NA #1,20NA #1,30NA
ILDP	-3,20UA			
IL1 IL2 IL3 IL4	-30,0UA -60,0UA -5,00UA -30,0UA			

RCA	CDP1822Sn	256 X 4	CMOS STATIC	RAM 31	AUG 78	TEMP:	85 C	SN:	3
		:·				PAGE	7 OF 10	71	

PASSED GALPAT PASSED GALPAT PASSED GALPAT (WIDE LIMITS) (TIGHT LIMITS) (TIGHT LIMITS) VCC=10V VCC=10V VCC=5V

PASSED DATA RETENTION TEST								
	vcc	≈ 4.5V	5'.øv	10.00				
ADDRESS ACCESS TIME	(TAA)	345.N	270'N	100 . N				
DATA SETUP TIME	(TDS)	18,ØN	16.0N	8 . 00 N				
DATA HOLD TIME	(TDH)	16.ØN	16.0N	14 . 0 N				
ADDRESS SETUP TIME	(TAS1)	6.90N	6 00N	4.00N				
ADDRESS SETUP TIME	(TAS2)	134.N	106 N	50.0N				
ADDRESS HOLD TIME	(TAH)	-16.0N	= 14 0N	-2.00N				
WRITE PULSE WIDTH	(TWP)	78.0N	70 0N	40.0N				
CS: SETUP TIME CS: SETUP TIME CS: HOLD TIME CS: HOLD TIME	(TCSS1)	166.N	144°N	76,0N				
	(TCSS2)	162.N	142°N	72,0N				
	(TCSH1)	46.0N	42°DN	28,0N				
	(TCSH2)	50.0N	46°DN	26,0N				
OUTPUT ACTIVE FROM COUTPUT ACTIVE FROM COUTPUT ACTIVE FROM ME	SE (TDOAE)	340.N 338.N 58.0N	276,N 272,N 50.0N	114.N 112.N 30.0N				
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDGH1) (TDGH2) (TDGH3) (TPGH) (TRC) (TWC)	158.N 154.N 144.N 142.N 368.N 224.N	126, N 122, N 122, N 116, N 288, N 200, N	40,0N 42,0N 36,0N 36,0N 128.N				
ĪIL	IIH	VIC1	AICS					
A0 =35.3NA	35.6NA	3.16 V	-3,14 V					
A1 =34.4NA	35.7NA	3.17 V	-3,19 V					
A2 =34.7NA	35.5NA	3.20 V	-3,24 V					
A3 =34.5NA	34.4NA	3.19 V	-3,22 V					
A4 #35,4NA	35,5NA	3.24 V	#3,27 V					
A5 #33,7NA	35.4NA	3.13 V	#3,16 V					
A6 #33,2NA	33,5NA	3.10 V	#3,15 V					
A7 #33.5NA	33,8NA	3.13 V	#3,16 V					
CS1 #35,6NA CS2 #34,3NA MWR #34,6NA MRD #35,1NA	33.9NA 36.1NA 34.2NA 35.2NA	3.22 V 3.24 V 3.18 V 3.21 V	-3,23 V -3,23 V -3,23 V					
DIØ =31.7NA	34.0NA	3.24 V	#3,19 V					
DI1 =32,5NA	34.1NA	3.23 V	#3,16 V					
DI2 =32,3NA	33.1NA	3.29 V	#3,22 V					
DI3 =32.9NA	35.7NA	3.24 V	#3,19 V					

RCA	COP1822SD	256	X 4	CHOS	STATIC	RAM	31	AUG 7	78
	000		001		מס	5		003	5
AOH 5 AOH 1 AOF 3	130.MV 130.MV 4.82 V 9.75 V		135 145 4.8 9.7	5 A WA	16! 4,8	73 V	·	168	5, HV 7, HV 32 V
IDN1 IDN2 IDN1	5.60MA 14.4MA =2.27MA =4.94MA		5.4 13.7 -2.2 -4.9	2 M A 4 M A	11 -2,	95MA 5MA 90MA 74MA			OMA OMA OMA OMA
1071 1072 1073 1074	8,50NA +2,20MA +4.30NA -4,60NA		19, 11. -2.0	9 N A 2 N A	#1,8 2.6	90NA 20NA 40NA 7.PA			
1025 1026 1027 1028	=9.70NA =6.60NA =9.50NA =6.20NA		1,40 3.20 990 1.70	PA	=4.8 =3.1 =4.6 =4.8	I ØNA 5 ØNA		-4-8 -3-8 -4-8	BONA Bona
ILDP	AU0.05								
IL1 IL2 IL3 IL4	+60,0UA +105.UA +40,0UA +65.0UA								

PAGE

#180.NA #183.NA #182.NA #184.NA

013 011 010

DI3

187,NA 189,NA 184,NA 190,NA

			PAG	E 9 OF 10
PASSED GALPAT (TIGHT	LIMITS) VO	C=10V C=10V C*5V	REPRODUCIBILITY ORIGINAL PAGE I	OF THE 3 POOR
PASSED DATA RETENTION	TEST			
	VCC	= 4.5V	5.øv	10.0V
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA) (TDS) (TDH)	340 N 18 ØN 18 ØN	275.N 16.0N 18.0N	110.N 8.70N 16.0N
ADDRESS SETUP TIME ADDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WIDTH	(TAS1) (TAS2) (TAH) (TWP)	2.00N 136.N -16.0N 82.0N	2.00N 112.N -12.0N 72.0N	4.70N 58.0N 44.0N
CS: SETUP TIME CS: SETUP TIME CS: HOLD TIME CS: HOLD TIME	(TCSS1) (SCSCT) (TCSH1) (SHCCT)	174.N 179.N 48.0N 52.0N	152', N 150. N 44. ON 46. ON	82,0N 78,0N 30,0N 38,0N
OUTPUT ACTIVE FROM CS OUTPUT ACTIVE FROM MRI	(SAOOT) S	354.N 352.N 60.GN	290, N 286. N 54. ØN	120.N 115.N 32.0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH1) (TDOH2) (TDOH3) (TPOH) (TRC) (TWC)	158 * N 154 * N 142 * N 144 * N 360 * N 232 * N	128, N 124, N 122, N 118, N 288, N 208, N	42,0N 44,0N 36,0N 38.0N 128.N 136.N
IIL	ITH	VICI	vica	
A1 =192.NA 1 A2 =194.NA	195.NA 192.NA 195.NA 192.NA	3.17 V 3.18 V 3.21 V 3.20 V	73,15 V 73,28 V 73,25 V 73,25 V	
A5 #189.NA 1	191,NA 192.NA 189,NA 189.NA	3.25 V 3.13 V 3.10 V 3.13 V	93,29 V 73,17 V 93,16 V 93,17 V	
CS2 =190,NA 1 MWR =193,NA 1	188,NA 196,NA 189,NA 189,NA	3.23 V 3.25 V 3.19 V 3.22 V	#3,24 V #3,25 V #3,21 V #3,25 V	

3.25 V 3,24 V 3.30 V 3.25 V

-3,17 V -3,23 V -3,20 V

RCA	COP1822SD	256	X	4	скоѕ	STATIC	RAM	31	AUG	78	TEMP:	125 C	SNt	3
											PAGE	10 OF	iØ	

	Doø	DO1	200	003
VOL 1	145.MV	150,MV	165.MV	160 MV
AOL'S	145.MV	160 MV		
VOH1			190.MV	180 MV
	4,80 V	4,80 V	4,80 V	4.81 V
SHOV	9.72 V	9.72 V	9.70 Y	9,72 V
IDNI	5.05MA	4'.90ma	4.50MA	4.65MA
IDNS	12,9MA	11.BMA	IØ.2MA	10.7MA
IDP1	-2,05MA	-2,04MA	-	TA WENT
IDP2			=1.99MA	₩2,05MA
TOPE	=4 47MA	~4.43MA	94,25MA	-4.51MA
TOZI	~456.NA	=429 NA	-439.NA	#451 NA
IOZZ	=483,NA	=442,NA	#460.NA	-452 NA
1023	-496.NA	-455.NA	#462,NA	-/146 kid
1024	=499 NA			≈466.NA
1024	en en d d B late	-452.NA	=471.NA	#465.NA
1025	∞500,NA	-455,NA	#466 NA	=471 NA
1026	#512.NA	≈450,NA	#472 NA	9473,NA
1027	-510.NA	#460,NA	9461 NA	유기 보고 기계 기계
IOZ8	-505,NA	=461.NA		9482 NA
2020	W N K C G C W	20 1 0 14 14 15	#473,NA	#472.NA
71 mm	em ¹ mile			
ILDP	65.ØUA			
IL1	≈190.UA			
11.2	#275.UA			
113	#145.UA			
11.4	⇔160.UA			

RCA CDP1822SD 256 X 4	CHOS STAT	IC RAM	31 AUG 78 TEMP	i 25 C SN:
			PAGI	1 OF 1M
		=10V		
	IMITS) VCC			
PASSED GALPAT (TIGHT L	IMITS) VCC	# ⊃ ¥		
PASSED DATA RETENTION TO	EST			
	vcc :	= 4.54	5'• ØV	10.0V
ADDRESS ACCESS TIME	(TAA)	270.N	220, N	90'. ØN
DATA SETUP TIME	(TDS)	18.ØN	16.0N	8.00N
DATA HOLD TIME	(TDH)	15,00	12.0N	12.00
AUDRESS SETUP TIME	(TAS1)	12.0N	10.0N	4 . ØØN
ADDRESS SETUP TIME	(TAS2)	128.N	106.N	48,0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-14,0N	-4.00N
WRITE PULSE WIDTH	(TWP)	66.0N	58. AN	36,0N
CS1 SETUP TIME	(TCSS1)	164.N	142, N	70,0N
CSS SETUP TIME	(TCSS2)	16Ø.N	138 N	68, ØN
CS1 HOLD TIME	(TCSH1)	34, ØN	30 . ON	22, ØN
CS2 HOLD TIME	(TCSH2)	38.ØN	34.0N	95.0N
OUTPUT ACTIVE FROM CS1	(TDDA1)	260.N	216,N	94, ØN
OUTPUT ACTIVE FROM CS2	(TDDA2)	258.N	214.N	92,0N
OUTPUT ACTIVE FROM MRD	(TDDA3)	54.0N	48.0N	26.0N
OUTPUT HOLD FROM CS1	(TDOH1)	158.N	126, N	38,0N
OUTPUT HOLD FROM CS2	(TOOH2)	154.N	182.N	38 ู้ ØN
OUTPUT HOLD FROM MRD	(T00H3)	146 . N	122, N 122, N	38,0N 34,0N
OUTPUT HOLD FROM MWR	(TPDH)	142,N	116 N	'40 £ SE
READ CYCLE TIME	(TRC)	272 N	อ≼อ_่ ผ	120 N

120.N 112.N

	nogo entre ewk	f EL (th.)	146,10	11.0 %
READ CY	CLE TIME	(TRC)	272 N	235°N
WRITE C	CYCLE TIME	(TWC)	304.N	216.N
		*******		E 5 C/ B / /
	9 4 1	TTI	line.	
	IIL	IIH	AICI	AICS
AØ	-2,40NA	2,60NA	5.99 V	-2,96 V
A1	MADE SH	1,90NA	3.04 V	-3.02 V
S A	=2.40NA	3.10NA	3_05 V	93,08 V
A B	-2.30NA	3.50NA	3.03 V	-3.06 V
.,_	H	m # m w w		-Dago V
A Ji	7 (QNA	7 00114	7 67 4	' T' 4 G U
A4	•3,10NA	3,00NA	3.07 V	-3,10 V
A 5	-2.50NA	5,20NA	3,00 V	-3.02 V
A6	-2.30NA	2,50NA	3.00 V	⊷3,02 V
A7	-2,30NA	2.10NA	3.01 V	-3.03 V
				- •
CS1	-2,50NA	2,20NA	7 07 V	-3,04 V
			3.03 V	m 3 - 10 4 V
CS2	42.70NA	2,50NA	3.05 V	-3,10 V
MWR	"2.70NA	2,50NA	3 00 V	+3,02 V
MRD	~2.90NA	3.00NA	3,02 V	-3.04 V
DIØ	#2.30NA	2,10NA	3.09 V	-3,04 V
DII	-2.80NA	2,30NA	3.08 V	-3,01 V
			•	
DIS	-2.60NA	2,60NA	3.10 V	-3,06 V
013	-2,60NA	2.50NA	3.11 V	≈3.06 V

RCA	CDP16228D	256 X 4	CMOS	STATIC	RAM	31	AUG	78	
	Doø	100		bas	2		DC	13	
VOL 2 VOL 2 VOH 2	115.MV 115.MV 4.85 V 9.79 V	120 120 4,8 9,8	.MV 5 V	140 4 _n 8	3, MV 3, MV 35 V 78 V		1747	5, MV 55, MV 85 V 85 V	
IDN1 IDN2 IDP1 IDP2	6,35MA 16.5MA ~2.63MA ~5,93MA	5.25 15.6 12.5 10.5	SMA Sma	5.7 13 =2.5			.14 ~2,	AMDB. AMDB. AMSB.	
1021 1022 1023 1024	18,5NA 15,0NA 13,3NA 16.9NA	11. 13. 15. 12.	6 N A 4 N A	10,	.5NA .7NA .6NA .9NA		18	8N8.3NA 2.3NA 2.2NA 2.9NA	
1025 1025 1027 1028	12,6NA 12,9NA 12,9NA 13,3NA	15 m 14 m 15 m 14 m	7NA 3NA	12,	3NA 1NA 0NA 6NA		14	1,4NA 1,1NA 1,5NA 1,9NA	
ILDP	-10.0UA								
IL1 IL2 IL3 IL4	-35,0UA -25,0UA -115,UA -35,0UA	•							

TEMP!

PAGE

SNI

a of vø

SN:

-20 C

PASSED GALPAT (TIGH	T LIMITS) VO	CC*10V CC*10V CC*5V	REPRODUCIBI ORIGINAL PA	LITY OF THE GE IS POOR
PASSED DATA RETENTIO	N TEST			
	vcc	: = 4,5Y	5 . øv	10.0V
ADDRESS ACCESS TIME	(TAA)	280 N	220 <u>.</u> n	10.0N
DATA SETUP TIME	(TDS)	22 0N	18.0n	8.00N
DATA HOLD TIME	(TDH)	10 0N	10.0n	80.0N
ADDRESS SETUP TIME	(TAS1)	16.0N	12.9N	4 - 00 N
ADDRESS SETUP TIME	(TAS2)	128.N	102.N	42 - 00 N
ADDRESS HOLD TIME	(TAH)	-18.0N	-14.0N	- 2 - 00 N
WRITE PULSE WIDTH	(TWP)	64.0N	56.0N	5 4 - 0 N
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS1)	160.N	136,N	66,0N
	(TCSS2)	156.N	134,N	64,0N
	(TCSH1)	32.0N	30.0N	20,0N
	(TCSH2)	38.0N	32.0N	18.0N
OUTPUT ACTIVE FROM COUTPUT ACTIVE FROM COUTPUT ACTIVE FROM M	SE (TDOAE)	266.N 264.N 50.0N	214 N 212 N 44 ON	88,0N 86,0N 84.0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME		150.N 146.N 142.N 138.N 256.N 248.N	116, N 114, N 120, N 14, N 192, N 200, N	34°00 36°00 32°00 32°00 112°0
IIL	IIH	VICI	VICS	
AD = 400.PA	400,PA	3.11 V	93,13 V	
A1 = 400.PA	300,PA	3.16 V	93,18 V	
A2 = 400.PA	700,PA	5.17 V	93,18 V	
A3 = 400.PA	800.PA	3.15 V	93,17 V	
A4 =700.PA	600 PA	3.19 V	-3,21 V	
A5 =400.PA	400 PA	3.12 V	-3,14 V	
A6 =400.PA	400 PA	3.13 V	-3,13 V	
A7 =400.PA	500 PA	3.13 V	-3,15 V	
CS1 =400.PA	400.PA	3,16 V	#3,16 V	
CS2 =500.PA	400.PA	3,17 V	#3,20 V	
MWR =600.PA	500.PA	3,13 V	#3,14 V	
MRD =600.PA	700.PA	3,15 V	#3,15 V	
010 +400.PA	300,PA	3.20 V	#3,15 V	
011 +500.PA	400.PA	3.20 V	#3,13 V	
012 +600.PA	500,PA	3.21 V	#3,17 V	
013 +500.PA	400.PA	3.23 V	#3,16 V	

RCA	COP182280	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMPi
					PAGE
	noø	001	500	003	
00H5 00H1 00F1	105.MY 100.MV 4.88 V 9.82 V	105 MV 105 MV 4 88 V 9 83 V	115.MV 120.MV 4.88 V 9.82 V	115.MV 115.MV 4.88 V 9.82 V	
1005 1005 1001	7.00MA 18.7MA -3.10MA -6.94MA	6.85MA 17.7MA ~3.08MA ~6.98MA	6.40MA 15.8MA 93.04MA 96.75MA	6,45MA 16,2MA 53,08MA 7,00MA	
1021 1022 1023 1024	3.80NA 1.40NA 8.60NA 6.50NA	5.10NA 8.00NA 900.PA 1.20NA	3.50NA 600.PA 6.70NA 6.10NA	3,70NA 7,10NA 1,30NA 800,PA	
1025 1026 1027 1028	1.80NA 2.10NA 1.80NA 1.90NA	6,70NA 7,00NA 6,70NA 6,70NA	300.PA -100.PA 400.PA 200.PA	7,40NA 7,20NA 7,40NA 7,20NA	
ILDP	-20.0UA				
IL1 IL3 IL4	~30,0UA ~15,0UA ~10,0UA ~UO,0E	·			

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SN:

PAGE 5 DF 10

PASSED GALPAT (WIDE LIMITS) VCC=10V PASSED GALPAT (TIGHT LIMITS) VCC=10V PASSED GALPAT (TIGHT LIMITS) VCC=5V

. Waste Dala utilities .	_ · · ·			
	vcc	# 4.5V	5	10.00
ADDRESS ACCESS TIME	(TAA)	PBØ.N	210'N	75 ON
DATA SETUP TIME	(TOS)			
		28, ØN	28.0N	a.poN
NATA HOLD TIME	(HOH)	10.0N	10.0N	10.0N
ADDRESS SETUP TIME	(TAS1)	12.0N	10.0N	4 . PAN
ADDRESS SETUP TIME	(TAS2)	126.N	100.N	40.0N
ADDRESS HOLD TIME	(TAH)	⊷18,0N	=14 g Ø N	-2.ŭ@N
WRITE PULSE WIDTH	(TWP)	66, ØN	56.0N	32,0N
CS1 SETUP TIME	(TCSS1)	158 _o N	134 N	62,gN
CS2 SETUP TIME	(TCSS2)	•		
		169.N	130 N	60,0N
CS1 HOLD TIME	(TESHI)	40, ØN	38.0N	ag, øN
CS2 HOLD TIME	(TCSH2)	42.0N	38 " ØN	18,00
OUTPUT ACTIVE FROM CS1	(TDOA1)	282.N	216, N	84° QN
OUTPUT ACTIVE FROM CS2	(SAGOT)	885*N	214.N	82,00
OUTPUT ACTIVE FROM MRD	(EAGGT)	48.ØN	48.0N	55, NM
OUTPUT HOLD FROM CS1	(TOOH1)	146.N	110 N	34, ON
OUTPUT HOLD FROM CS2	(трона)	142.N	(Ø.8. b)	32,0N
OUTPUT HOLD FROM MRD			108 N	
	(TDOH3)	142.N	118,N	30,0N
OUTPUT HOLD FROM MWR	(TPDH)	138,N	112.N	30.0N
READ CYCLE TIME	(TRC)	248,N	192 N 198 N	112.N
WRITE CYCLE TIME	(TWC)	256.N	145"N	96°0N
IIL II	H	VICI	VICP	
A0 -100.PA 10	Ø,PA	3.22 V	-3,19 V	
-	Ø PA	3.27 V	-3,25 V	
The state of the s	Ø.PA	3.28 V	-3 20 V	
	Ø.PA		-3,29 V	
A3 =100 PA 20	W e F A	3.27 V	=3.28 V	
	Ø, PA	3.30 V	-3,32 V	
	Ø.PA	3.24 V	-3,25 V	
A6 -100.PA 10	0,PA	3.23 V	#3,24 V	
A7 =100,PA 20	Ø.PA	3.24 V	#3,24 V #3,26 V	
CS1 -100.PA 10	Ø,PA	3_28 V	+3,27 V	
	Ø,PA	3.29 V	+3,31 V	
÷	Ø,PA	3,25 V	-3,25 V	
	Ø.PA	3.27 V	-3,26 V	
		_		
	0,PA	3.35 V	-3,26 V	
DI1 =100.PA 10	Ø.PA	3.31 V	#3,23 V	
	Ø.PA	3.32 V	-3,28 V	
	Ø.PA	3.35 V	-3.27 V	

RCA	CDP1822SD	256)	4	CHOS	STATIC	RAM	31	AUG	78
	BOA		001		מסמ	2		Dt	33
VOL 1	100.MV			.MV		S,MV		10	S MV
VOLE	90.0MV			ØWA		ð _# MV		19	MS.MV
ADH 7	4,89 V			9 y		39 V			,89 V
NOHS	9,85 V		9.8	5 Y	9,8	34 V		9.	.85 V
IDN1	7.55MA			ØMA	6.5	AMDE			AMON
IONS	20.5MA			5MA		.SMA			P. 9MA
IDP1	₩3.55MA		3,5		#3,6				57MA
IDP2	⇔7.99Mλ	-	8.0	4MA	#7.8	34MA		⇔ 8.	AMPO
TOZI	5,20NA			PA		50NA		. 1,	10NA
IOZ2	5.80NA	•	1,4	ONA		AMDE			40NA
IOZZ	-800.PA			ØN A		BONA		5,	70NA
1024	2.00NA		2.8	ØNA	₩ 1 Ø 0	PA		3,	SONA
1025	3,40NA		300	PΑ		AND		-10	10 PA
1026	3,00NA		800			50NA		=30	O PA
1027	3.20NA		500	•		20NA		. 10	10,PA
1028	3,00NA		900	"PA	3,8	PONA		ca 2 (10.PA
ILDP	=20.0UA								
ILi	-30,0UA								
IL2	⇒15,0UA								
IL3	⇔80,0UA								
11.4	-25.0UA								

TEMP:

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PASSED	GALPAT	(WIDE	LIMITS)	VCC=10V
PASSED		(TIGHT	LIMITS)	VCC=1ØV
PASSED	GALPAT	(TIGHT	LIMITS	VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION		2		
	vcc	= 4.5V	5.0V	10.0v
ADDRESS ACCESS TIME	(TAA)	260 "N	220'.	95.0N
DATA SETUP TIME	(TDS)	20 _p ØN	16.0N	8.00N
DATA HOLD TIME	(TDH)	16 • ØN	14.0N	14.0N
ADDRESS SETUP TIME ADDRESS SEYUP TIME ADDRESS HOLD TIME WRITE PULSE WINTH	(TAS1)	8.00N	6.00N	4.00
	(TAS2)	128.N	106.N	54.0N
	(TAH)	-18.0N	-14.00N	-4.00N
	(TWP)	78.0N	68.0N	40.0N
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS1)	168.N	148, N	76,0N
	(TCSS2)	166.N	144, N	74,0N
	(TCSH1)	44.ØN	40, AN	26,0N
	(TCSH2)	48.ØN	42, ON	26.0N
OUTPUT ACTIVE FROM CS	(SADOT) SE	256.N	218, N	106.N
OUTPUT ACTIVE FROM CS		252.N	216, N	104.N
OUTPUT ACTIVE FROM MR		58.ØN	50, ON	30.0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH1) (TDOH2) (TDOH3) (TPDH) (TRC) (TWC)	162.N 156.N 146.N 142.N 280.N 232.N	130°N 126°N 124°N 118°N 240°N 280°N	42,0N 42,0N 36,0N 38,0N 128,N
TIL	IIH	VICI	VICS	
AØ =29,0NA	30.1NA	2.93 V	#2,91 V	
A1 =29,7NA	27.7NA	2.98 V	#2,97 V	
A2 =29,4NA	31.3NA	2.99 V	#3,02 V	
A3 =28.9NA	33.7NA	2.97 V	#3,01 V	
A4 #31.8NA	31.3NA	3,01 V	23,95 V	
A5 #29.7NA	28.7NA	2.94 V	22,97 V	
A6 #29.1NA	29.2NA	2.94 V	2,96 V	
A7 #29.2NA	28.3NA	2.95 V	2,98 V	
CS1 #30.7NA	28.4NA	2.97 V	=2,99 V	
CS2 #31,0NA	30.9NA	3.00 V	=3,05 V	
MWR #29,1NA	29.9NA	2.95 V	=2,97 V	
MRD #32.0NA	31.4NA	2.97 V	=2,98 V	
DID =28,0NA	28.8NA	3.03 V	-2,98 V	
DI1 =30,5NA	28.8NA	3.02 V	-2,96 V	
DI2 =28.5NA	30.6NA	3.04 V	-3,01 V	
DI3 =28.5NA	28.8NA	3.05 V	-3,00 V	

RCA	CDP18225D	256 X 4 CMOS	STATIC RAM	31 AUG 78	ŤEMP i	85 C SNI
					PAGE	8 OF 10
	000	100	sod	003		
VOL1 VOH1 VOH1	130.MV 135.MV 4.82 V 9.74 V	140,MV 145,MV 4,82 V 9,75 V	150.MV 165.MV 4.72 V 9.74 V	145, MV 160. MV 4,82 V 9.75 V		
ION1 IDN2 IOP1 IOP2	5.55MA 14.0MA -2.23MA -4.99MA	5.40MA 13.2MA -2.21MA -4.99MA	5.70MA 11.7MA =2.14MA =4.76MA	5.05MA 12.1MA -2.19MA -5.01MA		
1021 1022 1023 1024	=16.3NA =31.4NA =34.2NA =34.4NA	-14,7NA -19,0NA -33,0NA -30,7NA	≈30,5NA ≈39,5NA ≈37,8NA ≈37,8NA	#23,8NA #25,2NA #36,9NA #35,6NA		
1025 1026 1027 1028	#39,6NA #37,2NA #39,9NA #37,7NA	-29,1NA -29,3NA -30,9NA -31,3NA	#45 0NA #43 4NA #44 5NA #41 9NA	934,6NA 932,7NA 935,0NA 933,6NA		
ILDP	50.ª0UV					
IL1 IL3 IL3 IL4	=65,0UA =60,0UA =145,UA =55,0UA					

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PASSED	GALPAT	(WIDE	LIMITS)	VCC=1ØV
PASSED	GALPAT	(TIGHT	LIMITS)	VCC=1@V
PASSED	GALPAT	(TIGHT	LIMITS)	VCC=5V

PASSEU DATA RETENTION	IESI			
	vcc	= 4 ₋ 5V	5'.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	27Ø.N	230'N	105.N
	(TDS)		16.0N	ละกดพ
DATA SETUE TIME		20,0N 16.0N		14.0N
DATA HOLD TIME	(HOF)	10 * 614	16. ON	14.00
ADDRESS SETUD TIME	(TAS1)	4.00N	4.00N	4.000
ADDRESS SETUP TIME	(TAS2)		112.N	60 ON
ADDRESS SETUP TIME ADDRESS HOLD TIME		132.N	#14 DN	
· · · · · · · · · · · · · · · · · · ·	(YAH)	#18,ØN		=4.70N 44.0N
WRITE PULSE WIDTH	(TWP)	82.ØN	72.0N	44 4 014
CS1 SETUP TIME	(TESS1)	176.N	156′ №	84 BN
CS2 SETUP TIME	(TCSS2)	172.N	152 ู้ N	82.ØN
CS1 HOLD TIME	(TCSH1)	46,0N	42 QN	58,0N 82,0N
CS2 HOLD TIME	(TCSH2)	50.0N	46.0N	28 ON
	(100110)			
OUTPUT ACTIVE FROM CS1	(TDOA1)	268.N	N,5ES	114.N
OUTPUT ACTIVE FROM CS2	(SADOT)	264.N	230.N	114.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	60 ON	54,0N	32,014
		W 25 B B		
OUTPUT HOLD FROM CS1	(TDOH1)	162.N	132°N	44 0 N
OUTPUT HOLD FROM CS2	(SHOOT)	158,N	128, N	44° ØN
OUTPUT HOLD FROM MRD	(TDOH3)	146 N	124 N	38 p Ø N
OUTPUT HOLD FROM MWR	(TPDH)	144.N	120 N	40.0N
READ CYCLE TIME	(YRC)	288.N	248 N	128.N
WRITE CYCLE TIME	(TWC)	240 N	216.N	136.N
		·- · - •/		22
IIL I	TH	VIC1	VTC2	
AØ #166,NA 16	61.NA	2.90 V	-2,88 V	
	59.NA	2,95 V	-2.94 V	
	65.NA	2.96 V	-2,94 V -3,00 V	
	67.NA	2.95 V	-2.99 V	
na samann ar	4 1 1 1 1 1 1	C /	_	
A4 -171.NA 16	66 , NA	2.99 V	-3'02 V -2'94 V -2'93 V	
-	60 NA	2.91 V	#2.94 V	
	59, NA	2.91 V	≂2.93 V	
A7 #164,NA 15	59 NA	2.93 V	#2 95 V	
CS1 #172.NA 15	59 NA	2.94 V	=2,96 V	
CS2 -168.NA 16	65,NA	2,97 V	#3,03 V	
	59,NA	2.91 V	-2,94 V	
MRD =171,NA 16	66 a N A	2.93 V	-2,95 V	
DIØ =160.NA 16	61 NA	3.00 V	-2,95 V	
	59.NA	3.00 V	#5.93 V	
	64.NA	3.01 V		
	61.NA	3.03 A	-2,98 V	
しゅつ かんごうりょく しょし	G L a IV M	A Ciner	-2.98 V	

RCA	CDP18225D	256 X 4	CHOS STATIC RAM	31 AUG 78	TEMPÍ	iás C sna	4
					PAGE	10 OF 10	

	DOØ	001	200	003
VOL 1	145.MV	150,MV	165.MV	165, MV
AOL'S	150 My	165.MV	185 MV	180 MV
VOH1	4.80 V	4.80 V	4.80 V	4,80 V
SHOV	9.72 V	9.72 V	9.71 V	9.72 V
IDNI	5.00MA	4.85MA	4.50MA	4.55MA
IDNE	12.5MA	11,8MA	10.4MA	19.7MA
IDP1	-2.00MA	-2.00MA	#1.94MA	-1,99MA
TOPE	#4.46MA	-4.50MA	#4.30MA	-4.47MA
1021	-622.NA	4568,NA	₩6Ø8,NA	-578, NA
1025	-655.NA	-592,NA	⇔620,NA	-592, NA
IOZ3	-673.NA	-600 kna	-634 NA	-598 NA
1024	#670.NA	-607.NA	#631.NA	#686.NA
1025	-672.NA	9603.NA	9633,NA	-607 NA
1026	-672.NA	-619.NA	e626 NA	-604, NA
YOZ7	₩673.NA	-613,NA	#631,NA	-593 NA
1028	-677.NA	-606.NA	-633,NA	#605.NA

ILDP	80'.0UA
ILI	#195,UA
115	-235 _m UA
11.3	-260.UA
IL4	⇔150,UA

RCA COP1822SD 256	X 4 CMOS STA	TIC RAM 3	1 AUG 78 TEMPi	as c sn:
			PÄGE	1 OF 10
	AT LIMITS) VO	C=10V C=10V C=5V		
PASSED DATA RETENTIO	N TEST			
	vcc	= 4.5V	5'. @V	10',0V
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA) (TDS) (TDH)	265.N 24,0N 12.0N	215.N 20.0N 10.0N	85.0N 8.00N 10.0N
ADDRESS SETUP TIME ADDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WIDTH	(TAS1) (TAS2) (TAH) (TWP)	12.0N 128.N -18.0N 72.0N	8.00N 102.N -14.0N 62.0N	4.00N 48.0N -4.00N 36.0N
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS1) (TCSS2) (TCSH1) (TCSH2)	168.N 166.N 40.0N 44.0N	142, N 140, N 36, AN 38, AN	55'0N 55'0N 66'0N 68'0N
OUTPUT ACTIVE FROM DUTPUT ACTIVE FROM DUTPUT ACTIVE FROM	(SADOT) SEC	252.N 248.N 54.0N	208, N 206. N 46. NN	56.4N 88.4N 88.4N
OUTPUT HOLD FROM CS OUTPUT HOLD FROM MR OUTPUT HOLD FROM MW READ CYCLE TIME WRITE CYCLE TIME	2 (TDOH2) C (TDOH3)	152 N 148 N 142 N 138 N 272 N	120,N 118,N 118,N 114,N 224,N 208,N	56,0N 36,0N 30,0N 32.0N 120.N 112.N
IIL	IIH	VICI	VIC2	
A0 ~2.20NA A1 ~1.80NA A2 ~2.30NA A3 #1.70NA	1.90NA 2.10NA 2.00NA 1.80NA	3.12 V 3.16 V 3.20 V 3.18 V	-3/12 V -3/18 V -3/20 V -3/20 V	
A4 #1,60NA A5 =1,70NA A6 #2,00NA A7 #1,50NA	2.20NA 2.10NA 2.10NA 2.10NA	3.19 V 3.09 V 3.10 V 3.10 V	-3,23 V -3,14 V -3,13 V -3,12 V	
CS1 =2,10NA CS2 =1,90NA MWR =1,80NA MRD =1,80NA	1,80NA 2,20NA 1,40NA 2,00NA	3.17 V 3.16 V 3.15 V 3.16 V	-3,15 V -3,17 V -3,18 V -3,17 V	
DIO +2.00NA DI1 #2.00NA DI2 #2.00NA DI3 #1.90NA	1,90NA 2,30NA 2,00NA 2,20NA	3.19 V 3.17 V 3.20 V 3.18 V	-3,14 V -3,12 V -3,16 V -3,14 V	

RCA	CDP18225D	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP
					PÄGE
	000	វ្និប្រជុំ	200	003	
AOH5 AOH7 AOF3	110,MV 110,MV 4,85 V 9,80 V	115 MV 120 MV 4 85 V 9 80 V	125,MV 135,MV 4,85 V 9,78 V	120, MV 130, MV 4,85 V 9,80 V	
IDN1 IDN2 IDP1 IDP2	6.80MA 17.3MA -2.64MA -6.01MA	6 45MA 15 9MA -2 63MA -5 96MA	AMQQ.2 AMP.E1 AMEE.S= AMB8.C=	6,05MA 14,3MA +2,61MA +5,96MA	
1021 1022 1023 1024	25,3NA 21,5NA 20,0NA 23,4NA	19.6NA 21.6NA 24.2NA 21.0NA	25,9NA 23,6NA 20,0NA 23.4NA	18,5NA 20,1NA 23,8NA 20,6NA	
1025 1026 1027 1028	19.5NA 19.6NA 19.5NA 19.6NA	24.3NA 23.9NA 24.4NA 23.4NA	21,4NA 21,3NA 21.0NA 21.1NA	21.9NA 22.1NA 21.7NA 22.0NA	
1LDP	≖800.ªNV				
IL1 IL2 IL3 IL4	-20,0UA -15,0UA -10,0UA -5,00UA				

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PASSED GALPAT PASSED GALPAT PASSED GALPAT	(WIDE LIMITS) (TIGHT LIMITS) (TIGHT LIMITS)	VCC=10V	REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR
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PASSED DATA RETENTION T	EST			
	vac	= 4.5V	5.0V	10°.00
ADDRESS ACCESS TIME	(TAA)	28Ø.N	215.N	75.0N
DATA SETUP TIME	(TDS)	28,01	55.WN	8.00N
DATA HOLD TIME	(HOH)	8.00N	8.001	10.0N
ADDRESS SETUP TIME	(TAS1)	16. ØN	12. ØN	4. PON
ADDRESS SETUP TIME	(TAS2)		100.N	42, ØN
ADDRESS HOLD TIME	(TAH)	128.N -18.0N	-14.9N	~2. @0N
WRITE PULSE WIOTH	(TWP)	68, ØN	48.0N	35,40
CS1 SETUP TIME	(TCSS1)	166 . N	138, N	62,0N
CS2 SETUP TIME	(TCSS2)	164.N	136 N	60,0N
CS1 HOLD TIME	(TCSH1)	40,0N	34.9N	55°0N
CSS HOLD TIME	(TCSH2)	44,0N	36.0N	20.0N
OUTPUT ACTIVE FROM CS1	(TOGA1)	258.N	506, N	82,0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	256.N	204.N	82 , ØN
OUTPUT ACTIVE FROM MRD	(TDNA3)	50.0N	42.9N	82,0N 24,0N
OUTPUT HOLD FROM CS:	(TDOH1)	146 N	114 N	34 pn
OUTPUT HOLD FROM CAZ	(SHOUT)	142.N	110, N	34,0N
OUTPUT HOLD FROM MRD	(TDOH3)	138.N	116 N	30,0N
OUTPUT HOLD FROM MWR	(TPDH)	136.N	112,N	30,0N
READ CYCLE TIMF	(TRC)	272,N	216 N	112.N
MRITE CYCLE TIME	(TWC)	264 a N	192'.N	104 a N
IIL II	Н	VICI	vica	
A0 -300.PA 30	Ø,PA	3.15 V	-3,15 V -3,21 V	
	Ø,PA	3,20 V	-3[21 V	
	Ø PA	3.23 V	#3,23 V	
A3 =300,PA 20	M.PA	3.21 V	-3.23 V	
A4 ~200,PA 30	Ø,PA	3.22 V	±3,25 V	
A5 +300.PA 40	Ø.PA	3.13 V	#3,18 V	
A6 9400 PA 30	Ø.PA	3.14 V	#3,18 V #3,17 V	
A7 =200,PA 30	21 . P A	3.14 V	-3.15 V	
CS1 =400.PA 300	Z _p P A	3.21 V	43,19 V	
	a μ P A	3.20 V	-3,21 V	
	Ø p P A	3.18 V	+3,21 V	
	2.PA	3.20 V	=3,20 V	
DIO =300 _e PA 300	Ø.FA	3.23 V	-3,18 V	
	Ø.PA	3.22 V	-3,16 V	
	Ø,PA	3,24 V	-3,29 V	
	Ø.PA	v ss.g	-3.18 V	

RCA	CDP182250	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMPI	#20 C	SN:
	·				PAGE	4 OF	10
	000	001	poz	003			
VOL1 VOH1 VOH2	95,0MV 95,0MV 4.88 V 9.83 V	100 MV 105 MV 4 88 V 9 83 V	110 MV 120 MV 4 88 V 9 82 V	110.MV 115.MV 4.88 V 9.82 V			
ION1 IDN2 IDP1 IDP2	7.50MA 19.6MA #3.12MA #7.07MA	7.20MA 18.2MA -3.09MA -7.03MA	6.70MA 16.0MA =3.03MA =6.76MA	6.75MA 16.5MA 33.10MA 77.07MA			
IOZ1 IOZ2 IOZ3 IOZ4		1,80NA 5,00NA 2.80NA 100,PA	6,50NA 2.90NA 3,70NA 7.40NA	800°PA 3°70NA 3°50NA 600°PA			
1025 1026 1027 1028	500.PA 500.PA 500.PA 600.PA	7.50NA 7.80NA 7.50NA 7.70NA	600,PA 500.PA 600.PA 500.PA	6,80NA 6,60NA 6,90NA 6.80NA	· .		
ILDP	-5.00UA						
YL1 YL2 YL3 YL4	#20,0UA #15,0UA #5,00UA #5,00UA						

VCC=5V

PASSED DATA RETENTION TEST

(TIGHT LIMITS)

L 11

	VC	C = 4.5V	5'_øv	10.0V
ADDRESS ACCESS TE	ME (TAA)	280 N	210'N	70.0N
PATA SETUP TIME	(TDS)	36. ØN	56 NV	8.00
DATA HOLD TIME	(TDH)	8 00N	8.00N	8.00N
			C • WVIII	0.00
ADDRESS SETUP TIM		16.0N	10.0N	4 . Ø0N
ADDRESS SETUP TIM		126.N	98.0N	38.ØN
ADDRESS HOLD TIME		=18,QN	=14.0N	⇔5°ធំចិស
WRITE PULSE WINTH	(TWP)	88, ØN	72.0N	30.0N
CS1 SETUP TIME	(TCSS1)	166 N	134 N	58,0N
CS2 SETUP TIME		166.N	1.34 a W	20 - NW
CS1 HOLD TIME	(TCSS2)	168 N	134 N	56, QN
	(TCSH1)	52,0N	36.PN	50°0N
CS2 HOLD TIME	(TCSH2)	54.0N	42 ₅ ØN	18.0N
OUTPUT ACTIVE FRO	M CS1 (TDOA1)	266.N	202, N	80,00
DUTPUT ACTIVE FRO		764.N	SOG.N	80,0N
OUTPUT ACTIVE FRO		48.2N	40.0N	22.00
	•		-	
OUTPUT HOLD FROM	CS1 (TDOH1)	142.N	1Ø8 ÅN	32,0N
OUTPUT HOLD FROM	CS2 (TDOH2)	138,N	104,N	32,00
OUTPUT HOLD FROM	MRD (TDOH3)	138 N	116 N	85. ØN
OUTPUT HOLD FROM	MWR (TPNH)	136,N	212,N	28,0N N0,85
READ CYCLE TIME	(TRC)	248 N	208,4	104.N
WRITE CYCLE TIME	(TWC)	248.N	192.N	96.0N
IIL	IIH	VICI	VICP	
AØ ≈100.PA	100,PA	3.22 V	-3,21 V	
A1 +100 PA	100,PA	3.26 V	-3,27 V	
A2 -100.PA	100,PA	3,29 V	-3,28 V	
A3 -100.PA	100.PA	3.28 V	-3.29 V	
	-			
A 4 0,00 A	100,PA	3.28 V	93,31 V	
A5 0.00 A	100,PA	3.19 V	Pa⊨eu v	
A6 =120,PA	100,PA	3,20 V	∞3.23 V	
A7 0.00 A	100.PA	3.20 V	₩3,21 V	
CS1 ~100.PA	100.PA	3.28 V	-3,25 V	
CS2 -100 PA	100 PA	3,27 V	TARES V	
MWR =100.PA	100,PA	3,25 V	+3,27 V +3,27 V	
MRD -100 PA	100.PA	3.27 V	#3 26 V	
- T #1 #1 B is Lz	↑ A2 A2 B4 M	3.07 ¥	т∂⊾⊈п V	
DIØ -100.P4	100.PA	3.29 V	=3,24 V	
DI1 =100.FA	100.PA	1.28 V	-3.22 V	
DI2 *100.PA	100,PA	3.31 V	-3,26 V	
DI3 -100.PA	100.PA	3.29 V	-3.24 V	

RCA	CDP1822SO	256 X 4 CMOS	STATEC RAM	31 AUG 78	TEMP
					PAGE
	DOB	001	pas	003	
AOH5 AOH1 AOL5 AOL1	90,0MV 85,0MV 4,89 V 9,85 V	95.0MV 95.0MV 4.89 V 9.85 V	100.MV 105.MV 4.88 V 9.84 V	100 MV 105 MV 4,89 V 9,85 V	
IDN1 IDN2 IDP1 IDP2	8 1 1 5 M A 21 1 6 M A 3 2 5 7 M A 8 1 1 M A	7,85MA 20,2MA -3,59MA -8,13MA	7.25MA 17.8MA 43.48MA 47.80MA	7.30MA 18.3MA 3.60MA 8.17MA	
10Z1 10Z2 10Z3 10Z4	100 PA 3.50NA 600.PA 1.40NA	4.10NA 400.PA 2.70NA 5.60NA	=900 PA 2 40NA 1 10NA -1 80NA	4,60NA 1,30NA 1,40NA 5,30NA	
1025 1026 1027 1028	6.00NA 5.70NA 5.90NA 5.50NA	-1,70NA -1,70NA -1,80NA -1,70NA	5.20NA 5.60NA 5.40NA 5.50NA	#1,30NA #1,50NA #1,50NA #1,60NA	
ILDP	=5.00UA				
IL1 IL2 IL3 IL4	#15,0UA #15,0UA #5,00UA #5,00UA				

SÑ:

6 OF 10

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90A CI	DP1822SD 256	X 4 CMOS	STATIC F	RAM 31 A	LUG 78	TEMP:	85 C SNI
						PAGE	7 OF 10
PASSED PASSED PASSED	GALPAT (TIGH	LIMITS) T LIMITS) T LIMITS)		y .	REPRODU ORIGINAL	CIBILITY O	f THE POOR
PASSED	DATA RETENTIO	N TEST					
			VCC = 4	. 5V	5.0V		10.0V
DATA S	S ACCESS TIME ETUP TIME OLD TIME	(TAA) (TDS) (TDH)	24	60.N 4.0N 2.0N	215'.1 20.01 12.0	Ŋ	90'.0N 8.00N 12.0N
ADDRES	S SETUP TIME S SETUP TIME S HOLD TIME PULSE WIDTH	(TAS1 (TAS2 (TAH) (TWP)	.) 8 2) 1; =1; 8;	. 20N 8, 0N 8, 0N	6.00 106.1 14.00 70.0	N	4 - 90N 54 - 9N 4 - 90N 40 - 9N
CS2 S	ETUP TIME ETUP TIME OLO TIME OLO TIME	(TCSS (TCSS (TCSF (TCSF	(2) 1 ¹	74.N 72.N 2.ØN 6.ØN	148, 146. 46.0 48.0	N	74'.0N 70'.0N 26'.0N 26'.0N
OUTPUT	ACTIVE FROM C ACTIVE FROM M	sa (TDOA	(2)	50 N 48 N 6 DN	214, 212. 50.0	N N	102.N 98,0N 28.0N
OUTPUT OUTPUT OUTPUT READ C	HOLD FROM CS1 HOLD FROM MRD HOLD FROM MWR YCLE TIME CYCLE TIME	(TDO)	12) 1 ³ 13) 1 1) 1	56 N 50 N 40 N 40 N 80 N	124r 120r 120r 114r 240r 208.	N N N	40,0M 40,0M 34,0M 34,0M 120,M
	TIL	IIH	AIC	1	AICS		
0A 11 22 24	-27,4NA -26,2NA -27,9NA -26,2NA	26.7NA 27.1NA 25.7NA 26.3NA	3,1 3,2 3,1	7 V 1 V	93,12 V #3,19 V #3,21 V #3,22 V		
A4 A5 A6 A7	#25,6NA #26,1NA #26,7NA #25,4NA	26.6NA 26.7NA 26.7NA 26.1NA	3.2 3.0 3.1 3.1	9 V 1 V	=3/24 V =3/14 V =3/14 V =3/12 V	•	
CS1 CS2 MWR MRD	=27,9NA =25,5NA =26,1NA =26,1NA	26.4NA 27.1NA 25.3NA 26.6NA	3.1 3,1 3.1 3.1	7 V 5 V	=3,16 V =3,19 V =3,19 V =3,15 V		

DIØ

DIT

DIS

DIN

-25,2NA

=24,8NA =24,5NA =24,9NA

25.4NA

26.9NA

26.4NA

26.6NA

3.19 V

3.18 V 3.21 V 3.19 V =3,14 V =3,13 V =3,17 V =3,15 V

RCA	CDP1822SO	ana x 4 chos	STATIC RAM	31 AUG 78	TEMPI	85 C	SN
					PAGE	8 0F 1	Ø
	იეთ	DO1	saa	003			
VOL 1	125.44	130.HV	140.MV	148, MV			
VOLE	125,47	140.MV	160 MV	155.HV			
VOHI	4.82 V	4,82 V	4.82 V	A RD V			
VOHE	9.76 V	9.76 V	9.74 V	4,82 V 9.76 V			
IUNI	5.95MA	5.65MA	5.20MA	5',25MA			
IDNS	14.9MA	13.6MA	11,9MA	AMS ST			
IDP1	AMES,S=	AMES,S+	#2.15MA	-2,21MA			
1065	#5.03MA	-5.03MA	-4.80MA	#5.01MA			
IOZ1	AM.SES	253 , NA	231.NA	235, NA			
IOZZ	225,NA	251,NA	233 NA	558,NY			
1023	227.NA	254,NA	AN _R EES	232,NA			
1024	225.NA	249.NA	237.NA	AN.855			
1025	225.NA	253 ₂ NA	A4.6ES	ANSES			
1076	235.NA	243,NA	243,NA	AN,SES			
IQZ7	233.NA	252,NA	AN.EES	241,NA			
1028	AM. 855	250.NA	241.NA	229 NA			
ILDP	≈5.00UA						
- 14 1	W D B C W						
IL1 IL2 IL3	≖35.0UA ≖40.0UA ≖25.0UA						
IL4	#20.0UA						

5

VCC=5V

PASSED DATA RETENTION TEST

PASSED GALPAT (TIGHT LIMITS)

	VCC	= 4.5V	5 . 0v	10.0V
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA) (TDS) (TDH)	265.N ?4,0N 14.0N	225.N 20.0N 14.0N	100.N 8.70N 14.0N
ADDRESS SETUP TIME ADDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WIDTH	(TAS1) (TAS2) (TAH) (TWP)	4.00N 139.N -18.0N 86.0N	4.00N 112'N -16.0N 76.0N	4.00N 60.0N ~4.00N 42.0N
CS1 SETUP TIME CSP SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS1) (TCSS2) (TCSH1) (TCSH2)	182,N 178,N 54,0N 58.0N	158'N 154'N 48, MN 50, MN	80,0N 78,0N 28,0N 28,0N
OUTPUT ACTIVE FROM CS1 OUTPUT ACTIVE FROM MRD	(TDOA1) (SAGGT) (TDOA3)	266.N 264.N 60.0N	230, N 226. N 54. AN	112.N 112.N 30.0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH1) (TDOH2) (TDOH3) (TPOH) (TRC) (TWC)	158 N 154 N 142 N 142 N 288 N 240 N	128, N 124, N 120, N 118, N 248, N 216, N	42,0N 44,0N 36,0N 128,N
IIF IIH		vici	VTCP	
A0 =163.NA 157 A1 =162.NA 159 A2 =167.NA 157 A3 =161.NA 156	, NA , NA	3.16 V 3.22 V 3.26 V 3.23 V	#3,16 V #3,24 V #3,26 V #3.27 V	
A4 =161.NA 157 A5 =161.NA 158 A6 =161.NA 157 A7 =158.NA 155	,NA ,NA	3,26 V 3,13 V 3,14 V 3,14 V	-3,30 V -3,19 V -3,18 V -3,16 V	
CS1 =168.NA 156 CS2 =160.NA 162 MWR =161.NA 155 MRD =160.NA 158	, NA , NA	5.22 V 5.21 V 3.20 V 3.22 V	~3,20 V ~3,24 V ~3,24 V ~3,23 V	
DIØ =153.NA 155 DI1 =154.NA 157 DI2 =150.NA 153 DI3 =150.NA 155	, N A . N A	3.24 V 3.22 V 3.25 V 3.23 V	-3,18 V -3,16 V -3,21 V -3,19 V	

RCA	CDF1822SD	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMPS	125 C S
		•			PAGE	10 OF 10
	DOO	001	במת	003		·
AOF5 AOF5 AOF7	140.MV 145.MV 4.80 V 9.72 V	145 MV 160 MV 4,80 V 9,72 V	160.MV 180.MV 4.80 V 9.71 V	160 MV 175 MV 4 80 V 9 72 V		
IDN1 IDN2 IDP1	AM25.6 AM5.81 AM00.5-	5.05MA 12.1MA -2.01MA -4.53MA	4.70MA 10.6MA +1.94MA +4.30MA	4.75MA 10.9MA -1.99MA -4.49MA		
10F2 1071 1072 1073 1074	1.09UA 1.07UA	1,13UA 1,13UA 1,13UA 1,13UA	1.10UA 1.08UA 1.09UA 1.09UA	1,05UA 1,06UA 1,05UA 1,05UA		
1025 1026 1027 1028	1.08UA 1.09UA 1.09UA	1,14UA 1,14UA 1,13UA 1,14UA	1.11UA 1.11UA 1.10UA 1.00UA	1,07UA 1,06UA 1,06UA 1,07UA		
ILDP	40.0UA					

IL1 IL2 IL3 IL4 #110.UA #120.UA #100.UA #80.0UA SNS

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RCA	CDP182250	256 X 4	CMOS	STATIC RA	M 31	AHG	78	TEMP:	25 (:	SN:	6
								DICE	• 0:			

PASSED	GALPAT	(WIDE	LIMITS	VCC=10V	
PASSED	GALPAT	(TIGHT	LIMITS)	VCC=10V	REPRODUCIBILITY OF THE
PASSED	GALPAT	тнашт)	LIMITS)	VCC=5V	ORIGINAL PAGE IS POOR

	VCC	= 4.5V	5'.øv	10.0V
AUDRESS ACCESS TIME	(TAA)	325.N	255 N	85.0N
DATA SETUP TIME	(TOS)	30,0N	54°0V	8 . 00N
DATA HOLD TIPE	(roH)	12.0N	10.70	10.00
ADDRESS SETUP TIME	(YAS1)	10.0N	8,07N	4.00N
ADDRESS SETUP TIME	(TAS2)	142.N	114.N	48.0N
ADDRESS HOLD TIME	(TAH)	-26, ON	∞50°0N	-4.00N
WRITE PULSE WINTH	(TWP)	78.ØN	68 ª WN	36,0N
CS1 SETUP TIME	(TCSS1)	188.N	154, N	68, ØN
CSS SETUP TIME	(TCS52)	182.N	150.N	66,0N
CSI HOLD TIME	(TCSH1)	50,0N	42 . an	24,0N
CSS HOLD TIME	(TCSH2)	54.CN	46. Mr.	24 . ON
OUTPUT ACTIVE FROM CS1	(TOGA1)	294.N	236, N	94 ู้ อูฟ
OUTPUT ACTIVE FROM CS2	(SAPOT)	5 à bi " N	235 N	94, ØN
OUTPUT ACTIVE FROM MRD	(TDOA3)	60.0N	52.0N	26.0N
OUTPUT HOLD FROM CS1	(TDOH1)	162.N	130, N	40', 0N
OUTPUT HOLD FROM CS2	(SHOOT)	158.N	126.N	42,0N
OUTPUT HOLD FROM MRO	(10043)	144.N	120,1	30,0N
OUTPUT HOLD FROM MWR	(ዝብዓፕ)	142.N	118,N	32,0N
READ CYCLE TIME	(TRC)	328 N	264, N	120.N
WRITE CYCLE TIME	(TWC)	272.N	272.N	112.N
IIL	IH	VICI	VICP	
AØ =37,5NA 2,	,20NA	3.39 V	-3,38 V	
A1 =2.20NA 2	, BØNA	3.41 V	41 V 44 م3 m	
	, 20NA	3.44 V	43,45 V	
A3 -2,50NA 2	.60NA	3.45 V	-3,47 V	
A4 -10.3NA 2.	. 40NA	3.46 V	-3,47 V	
AS #2.30NA 2,	,40NA	3.35 V	-3,59 V	
	,30NA	3.37 V	-3,41 V	
	.60NA	3.39 V	-3.40 V	
	,50NA	3.42 V	+3,44 V +3,44 V +3,38 V	
CS2 =2.40NA 3.	10NA	3.41 V	#3,44 V	
	, 60NA	3.38 V	•3 58 V	
	ZONA	3.38 V	=3.39 V	
	40NA	3.52 V	+3,46 V	
	, 40h, A	3.51 V	-3,44 V	
DI2 -2,40NA 2,	, 10NA	3.48 V	-3,44 V	
DI3 =2.40NA 2.	.3MNA	3.48 V	-3,42 V	

RCA	CDP1822SD	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP!	25 C	SNI
					PAGE	2 OF	10
	Dog	100	pos	D03	`		
AOH3 AOH1 AOFS AOF1	125.MV 120.MV 4.83 V 9.77 V	130,MV 130,MV 4,83 V 9,77 V	140,MV 150,MV 4,82 V 9,76 V	140 MV 145 MV 4,82 V 9,77 V			
ION1 ION2 IOP1 IOP2	5.75MA 15.7MA -2.28MA -5.41MA	5.55MA 14.5MA -2.27MA -5.45MA	5.25MA 13.0MA -2.23MA -5.24MA	5,20MA _13,0MA =2,25MA =5,41MA			
1021 1022 1023 1024	44.8NA 44.1NA 49.7NA 46.2NA	54,3NA 53,9NA 47.7NA 50.3NA	51,6NA 49,8NA 56,9NA 53,9NA	74,1NA 75,4NA 66,1NA 82,7NA			
1025 1076 1027 1028	46,0NA 46.6NA 46.0NA 45.9NA	51.7NA 52.2NA 52.2NA 51.9NA	53,2NA 52,3NA 51,6NA 51.0NA	85.9NA 72.8NA 73,3NA 72.4NA			
ILOP	-10.0UA						
YL 1 IL 2 IL 3 IL 4	⇔60.0UA ⇔115.UA ⇔40,0UA ⇔95.0UA						

PASSED GALPAT (WIDE LIMITS) VCC=10V PASSED GALPAT (TIGHT LIMITS) VCC=10V PASSED GALPAT (TIGHT LIMITS) VCC=5V

Harries Barry	······································	-,			•	
		vcc	= 4.5V	5.0	ν	10.0V
ADDRESS ACCES	SS TIME	(TAA)	385.N	270	r. Ni	80.00
DATA SETUP T		(TOS)	•			
			36,0N			8.00N
DATA HOLD TI	l.₌ Ĺ	(TDH)	10.0N	8,0	N N	10.0N
ADDRESS SETUI	P TIME	(TAS1)	18,0N	14.	ØΝ	4.00N
ADDRESS SETU	P TIME	(TAS2)	162.N			44 ØN
AUDRESS HOLD	TIMF	(TAH)	-26 ON	-2A.		4 . P. Q.N
WRITE PULSE	· •	(TWP)	94.0N			36 ØN
ee, cerun	T + Mc.	1800013	200 1	4 5 4	• .	4 11 AN
_	TIME	(TCSS1)	208.N		<u> </u>	64 ØN
CS2 SETUP		(TOSSE)	50¢*N		■ N	62,0N
	TME	(TCSH1)	44, ØN		an	22,ØN
CSS HOLD T	TMF	(TCSH2)	50.QN	42.	۵N	55.0M
OUTPUT ACTIV	E FROM CS1	(TOOA1)	326.N	242	r _ Ni	88,ØN
OUTPUT ACTIV		(SADOT)	4,52E	242	r ki	BA AN
OUTPUT ACTIVI		(TDDA3)	58.0N		R IT ZI ki	86,0N 24,0N
ODI, DI ACITA	r. i perior eroge	() DOM 3)	30 * 8 W	·		·
OUTPUT HOLD !	FROM CSi	(TDOH1)	158.N	124	N	38 ØN
OUTPUT HOLD I	FROM CS2	(TD0H2)	154.N		_ N	38. NN
PUTPUT HOLD !	FROM MRD	(TDOH3)	142.N		N	30 DN
OUTPUT HOLD		(TPDH)	142.N	· ·	N	30 0N 30 0N
READ CYCLE T		(TRC)	320 N		F N	104 N
WRITE CYCLE		(TWC)	288 N	304	P N	
HILL GIOCE	1 L 12.	(MC)	7 O O ⊕ N	34.4	a 17	104.N
IIL	ITH		VICi	VICE		
AØ -13,41	NA 300	. P A	3.43 V	-3,42	٧	
A1 #200.	PA 500	PΑ	3.46 V	-3.45	V	
A2 #300.1	PA 300,	.PA	3.49 V			
A3 #300.1			3.50 V	-3,49 -3,51	V	
A4): A 200	D.A.	7 60 U	يُ سو ٿو		
A4 -2,201			3,50 V	*	V	
A5 =300.	•		3,40 V		V	
A6 ≈300,1		, P A	3.42 V		V	
A7 -500.1	P	_ P A	3.43 V	-3.45	V	
CS1 =400.1	PA 400;	PΔ	3.47 Y	#3,48	ν	
CS2 =300.	PA 600		3.47 V	±3,48		
MWR =300.1			3.43 V	-3,43		
MRD #300.			3.43 V	+3.43		
THE THE STATE OF T	14161	9 t P4	ን ዶ ሣጋ ¥		Y	
DI0 +300.	PA 300.	.PA	3.57 V	-3,50	V	
DI1 =300.		.PA	3.56 V	=3,48	٧	
DIS ~300.1			3.53 V	-3,48	V	
DI3 =400.	•		3.53 V	-3.47		
	. 5.00	• •			*	

RCA	CDP18225D	256 X 4	CMOS	STATIC	RAM	31	AUG 78	TEMP	e 20	C	SN:	6
								PAGE	4 0	F 12	9	

	Doø	001	005	003
A0H5 A0H1 A0F3	120.MV 105.MV 4.86 V 9.80 V	120, MV 115, MV 4, 85 V 9,81 V	130.MV 130.MV 4.85 V 9.80 V	130 MV 150 MV 4786 V 9.81 V
ION1	6.20MA	6.00MA	5.70MA	5,65MA
ION2	17.6MA	16.3MA	14.6MA	14,8MA
IOP1	=2.68MA	-2.67MA	#2.61MA	12,63MA
IOP2	=6.40MA	-4.48MA	#6.15MA	16,40MA
1021	7,00NA	7.80NA	8.90NA	13.8NA
1022	4,00NA	11.0NA	5.40NA	20.5NA
1023	10,7NA	4.80NA	11.3NA	17,9NA
1024	9,60NA	4.70NA	11.6NA	15.0NA
1025	4.10NA	11,1NA	5.10NA	22,0NA
1026	3.90NA	10,9NA	5.30NA	24,2NA
1027	4.00NA	11.3NA	5.10NA	22,6NA
1028	3.80NA	11,0NA	5.10NA	22,9NA

IL	ŊΡ	m 2	٠.	Bı	ØŪ	۸
A 100	~ 1	7-6	. •	.,,	,	r٠

IL1 #50,0UA IL2 #95,0UA IL3 #30,0UA IL4 #75,0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V PASSED GALPAT (TIGHT LIMITS) VCC=10V PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

	vec	= 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA) (TDS) (HDT)	415.N 50.0N 6.00N	270'.N 34.0N 6.00N	75.0N 8.00N 8.00N
ADDRESS SETUP TIME ADDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WIDTH	(TAS1) (TAS2) (TAH) (TWP)	16.0N 172.N 28.0N 112.N	12.0N 116.N =20.0N 84.0N	4.00N 40.0N +2.00N 36.0N
CS: SETUP TIME CS: SETUP TIME CS: HOLD TIME CS: HOLD TIME	(TCSS1) (TCSS2) (TCSH1) (TCSH2)	238.N 236.N 48.ØN 74.ØN	154°N 156°N 52°N 52°N	55.60 55.60 66.60 5.00 8.00
OUTPUT ACTIVE FROM CS1 OUTPUT ACTIVE FROM MRD	(TDOA1) (TDOA2) (TDOA3)	366.N 364.N 54.ON	246, N 244. N 46. GN	55.0N 85.0N 85.0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH1) (TDOH2) (TDOH3) (TPOH) (TRC) (TWC)	154.N 148.N 140.N 140.N 336.N 288.N	118 N 116 N 118 N 114 N 240 N 224 N	38,0N 36,0N 28,0N 30,0N 104.0N
11r I.	IH	VICI	AICS	
A1 =100.PA 20 A2 =100.PA 10	00.PA 00.PA 00.PA 00.PA	3.51 V 3.53 V 3.56 V 3.58 V	#3,49 V #3,52 V #3,56 V #3,59 V	
A5 =100.PA 10	00.PA 00.PA 00.PA 00.PA	3.58 V 3.47 V 3.49 V 3.50 V	=3.58 V =3.51 V =3.52 V =3.52 V	
CS2 *100.PA 20 MWR =100.PA 10	20, PA 70, PA 20, PA 20, PA	3.55 V 3.55 V 3.51 V 3.51 V	#3,56 V #3,55 V #3,51 V #3,51 V	
DI1 =100.PA 10	20, PA 20, PA 70, PA 70, PA	3.64 V 3.63 V 3.60 V 3.61 V	-3,57 V -3,55 V -3,56 V -3,54 V	

RCA	CDP1822SD	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP	-55 C	SNI	6
					PAGE	~6 OF	10	
	000	001	DO.S	D03				
AOH 5 AOM 7 AOM 7 AOM 7	4,88 V	115,MV 105,MV 4,88 V 9,84 V	125.MV 120.MV 4.88 V 9.83 V	125, MV 115, MV 4, 88 V 9,84 V				
IDN1 IDN2 IDP1 IOP2	6,60MA 19,2MA =3,03MA	6.35MA 17.8MA -3.05MA -7.43MA	6.05MA 16.1MA =3.00MA =7.14MA	5.95MA 16.1MA -3.00MA -7.38MA				
IUZ1 IOZ2 IOZ3 IOZ4	-100.PA 3.10NA 2.60NA	5,60NA 2,30NA 1,30NA 5,00NA	₩600.PA 1.90NA 3.60NA 300.PA	11.9NA 9,20NA 6.70NA 10.4NA				
1025 1026 1027 1028	4.90NA 4.30NA	300.PA 500.PA 600.PA 900.PA	4.10NA 3.60NA 3.70NA 3.10NA	7,800A 7,100A 4,700A 7.300A				
ILDP	∞2.40UA					¢		
IL1 IL2 IL3 IL4	-45,0UA -90,0UA -25,0UA -70,0UA							

PAGE 7 OF 10

PASSED	GALPAT	(TIGHT	LIMITS) LIMITS) LIMITS)	VCC=10V	REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR
PASSED	DATA RET	ENTION	TEST		
					,

	VCC	= 4.5V	5',øv	10.0V
AUDRESS ACCESS TIME DATA SETHP TIME DATA HOLD TIME	(TAA) (TDS) (HDH)	895.N 32,0N 12.0N	240 <u>'</u> N 24.0N 12.0N	95,0N 8.00N 95,0N
ADDRESS SETUP TIME ADDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WIDTH	(1281) (2821) (441) (441)	6.00N 136.N -24.0N 92.0N	6.09N 112.N =18.0N 78.0N	4.00N 54.0N -4.00N 42.0N
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS1) (TCSS2) (TCSH1) (TCSH2)	192.N 188.N 60,0N 62.0N	160'N 158'N 52'0N 54'0N	74,0 72,0 72,0 30,0 30.0
OUTPUT ACTIVE FROM CS1 OUTPUT ACTIVE FROM CS2 OUTPUT ACTIVE FROM MRD	(TDDA1) (TDBA2) (TDBA3)	278.N 274.N 62.ØN	232, N 230. N 54. MN	104.N 104.N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH1) (TDOH2) (TDOH3) (TPOH) (TRC) (TWC)	162.N 158.N 142.N 142.N 320.N 248.N	130, N 126, N 126, N 118, N 264, N 216, N	42,00 42,00 44,00 120,00 120,00 120,00
IIL I	IH	AICI	VICS	
A1 #31,3NA 3' A2 #30,8NA 30	0.8NA 1,9NA 0.3NA 2.2NA	3.39 V 3.41 V 3.44 V 3.46 V	=3,38 V =3,41 V =3,45 V =3,48 V	
A5 #31,5NA 31	0.1NA 1.3NA 1.2NA 1.6NA	3,46 V 3,35 V 3,38 V 3,39 V	-3,48 V -3,39 V -3,41 V -3,41 V	
CS2 =30,7NA 3: MWR =30,8NA 3:	0.4NA 3.2NA 0.5NA 0.1NA	3,42 V 3,41 V 3,38 V 5,38 V	-3,44 V -3,44 V -3,38 V -3,39 V	
DI1 #30,5NA 30	1.0NA 0.9NA 9.8NA 9.8NA	3.53 V 3.51 V 3.48 V 3.48 V	93,47 V 93,44 V 93,44 V 93,43 V	

RCA	CDP1822SD	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMPI	85 C	SNI	6
					PAGE	8 OF	iõ	
	DOØ	DOi	šoa	003				
VOL 2 VOL 2 VOH 1	140.MV 140.MV 4.80 V 9.73 V	150 MV 150 MV 4,80 V 9,73 V	160.MV 175.MV 4.80 V 9.72 V	160 MV 170 MV 4 80 V 9 72 V				
ION1 IDN2 IDP1 IDP2	5.20MA 13.6MA -1.96MA -4.58MA	4,95MA 12.5MA -1,93MA -4,59MA	4.70MA 11.1MA -1.91MA -4.43MA	4.65MA 11.5MA 11.92MA 4.58MA				
1021 1022 1023 1024	373.NA 376.NA 370.NA 372.NA	394 NA 389 NA 388 NA 390 NA	414 NA 405 NA 408 NA 402 NA	416 NA 434 NA 425 NA 448 NA				
1025 1026 1027 1028	376.NA 366.NA 369.NA 371.NA	393', NA 404, NA 390, NA 398, NA	411,NA 405,NA 413,NA 403.NA	432° NA 449° NA 431° NA 436° NA				
ILOP	-5,00UA							
IL1 IL2 IL3 IL4	-90,0UA -150,UA -70,0UA -125,UA							

PASSED	GALPAT	CMIDE	LIMITS)	VCC=10V
PASSEL	GALPAT	(TIGHT	LIMITS)	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS)	VCC#5V

I MODI D DAIN WEITHITON	1.01			
	VCC	= 4,5V	5. ØV	10.0V
ADDRESS ACCESS TIME	(TAA)	285.N	240.N	105.N
DATA SETUP TIME	(BOT)	30,0N	24.0N	8 . ØØN
DATA HOLD TIME	(нат)	12,0N	12.0N	15.0N
ADDRESS SETUP TIME	(TAS1)	2,000	a. aan	4 . P.O.N
ADDRESS SETUP TIME	(TAS2)	136.N	120.N	62.UN
ADDRESS HOLD TIME	(HAT)	-22,0N	-18 0N	-6.PEN
WRITE PULSE WIDTH	(TWP)	94.0N	B2.NN	44.0N
CS1 SETUP TIME	(TCSS1)	190.N	164 N 160 N	80,0N
CS2 SETUP TIME	(TCSS2)	186.N	1.5 M	78, ØN
CS1 HOLD TIME	(TCSH1)	64, ØN	54 g/N	30, QN
CS2 HOLD TIME	(TCSH2)	66.0N	56,AN	30.0N
pot noth trui	(TGGHE)	tin # Ai⊿	·	20.00
OUTPUT ACTIVE FROM CS1	(TDDA1)	284.N	244, N	118.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	280 N	240 N	114.M
OUTPUT ACTIVE FROM MPD	(TUUA3)	62.0N	54.0N	30.0N
OUTPUT HOLD FROM CS:	(TDDH1)	160.N	130 N	46 ØN
OUTPUT HOLD FROM CS2	(TDOH2)	156,N	126,N	46, UN
OUTPUT HOLD FROM MRD	(TDOH3)	140 N	120,N	46, ØN 36, ØN
OUTPUT HOLD FROM MWR	(TPNH)	144.N	118.N	36.0N
READ CYCLE TIME	(TRC)	320.N	264, N	128.N
WRITE CYCLE TIME	(TWC)	N.SES	216.N	128.N
				•
TIL II	H	VICI	ALCS	
AØ =403.NA 17	4.NA	3.42 V	-3,41 V	
	3.NA	3.44 V	-3.44 V	
	2.NA	3.48 V	#3,44 V	
	5.NA	3.49 V	43 52 V	
	5,NA	3,49 V	-3,52 V	
	'4 _μ ΝΑ	3.38 V	₩3,42 V	
A6 +179.NA 17	'5 NA	3.40 V	-3.44 V	
A7 =179.NA 17	2.NA	3.43 V	-3.44 V	
CS1 -170.NA 16	7, NA	3,45 V	=3,47 V	
	6.NA	3.44 V	#3,48 V	
	4,NA	3.40 V	-3,41 V	
· · · · · ·	4.NA	3.40 V	3.42 V	
- · · ·		7645 A		
DIO -171.NA 17	4-NA	3.56 V	-3,50 V	
	'2°NA	3.55 V	#3,48 V	
	4 NA	3,52 V	≈3,48 V	
	16.NA	3,52 V	-3.46 V	
			- ·	

RCA	CDP1822SD	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP	125 C
			•		PAGE	18 OF 16
	000	D01	sod	003		•
VOL1 VOL2 VOH1	155.MV 155.MV 4.78 V 9.69 V	165,MV 170,MV 4,78 V 9,69 V	175.MV 195.MV 4.77 V 9.68 V	175 MY 190 MY 4,77 V 9.69 V		
IDP2 IDP1 IDN1	4.75MA 12.2MA =1.78MA =4.13MA	4,55MA 11,3MA =1,77MA =4,13MA	4.30MA 10.0MA #1.73MA #3.99MA	4.25MA 10.1MA 17.75MA 41.13MA		
IOZ1 IOZ2 IOZ3 IOZ4	AUEE.1 AUPE.1 AUWE.1 AUPS.1	1,40UA 1,40UA 1,39UA 1,39UA	1.44UA 1.42UA 1.43UA 1.42UA	1,42UA 1,42UA 1,40UA 1,40UA		
1075 1076 1077 1078	1.31UA 1.31UA 1.30UA 1.29UA	1,40UA 1,40UA 1,39UA 1,40UA	1.45UA 1.44UA 1.43UA 1.42UA	1,44UA 1,44UA 1,43UA 1,44UA		
ILDP	50 <u>.</u> 0UA					
IL1 IL2 IL3 IL4	≈185.UA ≈265.UA ≈165.UA ≈205.UA					

SNi

en e	e as a second and a second and the s	-	
RCA CDP1822SD 256 X 4	CHOS STATIC RA	M 31 AUG 78 TEMP	i as c ani
		PÁG	E 1 OF 10
The state of the s	IMITS) VCC=10V		
PASSED GALPAT (TIGHT L' PASSED GALPAT (TIGHT L'		REPRODUCIBILITY ORIGINAL PAGE	
PASSED DATA RETENTION TO	EST	ORIGINAL FAGE	.b 1001;
	VCC = 4.5	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA) 285	· ·	95'.ØN
DATA SETUP TIME DATA HOLD TIME	(TDS) 24,0 (TDH) 12.0		12.0N 12.0N
ADDRESS SETUP TIME	(TAS1) 14	3N 12.PN	4_ 7 0N
ADDRESS SETUP TIME	(TAS2) !34	N 108 N	52.0N
ADDRESS HOLD TIME WRITE PULSE WIDTH	(TAH) =20% (TWP) 76%	8N =16.0N 8N 62.0N	-4.60N 38.6N
CS1 SETUP TIME	(TCSS1) 178		76, ØN
CS2 SETUP TIME CS1 HOLD TIME	(TCSS2) 174 (TCSH1) 38,	,N 150°,N	74.0N
CS2 HOLD TIME	(TCSH2) 40.	#N 36.0N	22 . 0%
OUTPUT ACTIVE FROM CS1	(TDOA1) 266	_	109.N
OUTPUT ACTIVE FROM CS2 OUTPUT ACTIVE FROM MRD	(TDOA2) 264.	'N 550'N	98,0N 28,0N
	1 CENTRAL TO	•	SO BM
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM CS2	(TDOH1) 152,		34,0N
OUTPUT HOLD FROM MRD	(TDOH2) 148, (TDOH3) 138,		34 8N
OUTPUT HOLD FROM MWR	(TPDH) 138,		36,0N 36,0N
READ CYCLE TIME	(TRC) 288,	- - -	128 N
WRITE CYCLE TIME	(TWC) 240.	N 208,N	158 N

	IIL.	IIH	VIC1	vice
ΑØ	=1.30NA	1.50NA	2.93 V	-2,91 V
A 1	-1.50NA	1,80NA	86 S	-3,00 V
45	-1.40NA	1,40NA	2.99 V	=3,01 V
EA	-1.70NA	1.49NA	ä. 97 v	-3.02 V
A4	-1.30NA	1.40NA	3.01 V	-3,02 V
A5	-1.80NA	1.80NA	8 98 V	2 94 V
A6	-1.70NA	1.40NA	2.94 V	-2,96 V
A7	-1.40NA	1.70NA	2.94 V	-2.94 V
CS1	=1.50NA	1,40NA	2.93 V	_2 05 V
CSZ	-1.80NA	1.30NA	2.96 V	-2,95 V -2,99 V
MWR	-1.70NA	1.50NA	2.93 v	-2,98 V
MRD	-1.50NA	1.90NA	2 93 V	=2.94 V
DIØ	-2.20NA	1.40NA	3.03 V	-2'.98 V
DII	≈1.70N A	1.40NA	3.02 V	-2,96 V
DIS	-1.60NA	1.50NA	3.01 V	-2,97 V
DIB	-1.70NA	1.30NA	3.90 V	-2.97 V

RCA	COP1822SD	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP:	25 C SN:
					PAGE	2 OF 10
	DOG	DO1	څوه	D03		
VOL1 VOH1 VOH2	115.MV 115.MV 4.84 V 9.77 V	120,MV 130,MV 4,84 V 9,77 V	125.MV 145.MV 4.84 V 9.76 V	125, MV 135, MV 4,84 V 9,77 V		
IDN1 IDN2 IDP1 IDP2	6.35MA -16.0MA -2.40MA -5.33MA	6.10MA 14.9MA -2.42MA -5.39MA	5.85MA 13.4MA =2.37MA =5.24MA	5,95MA 13,9MA -2,44MA -5,47MA		
1021 1022 1023 1024	34.6MA 34.2NA 27,8NA 30.2NA	27.8NA 26.2NA 32.8NA 30.3NA	34,5NA 36,2NA 29,2NA 30.8NA	30,5NA 30,3NA 40,35 30,3NA		
1025 1026 1027 1028	32.0NA 32.3NA 32.0NA 31.7NA	27.7NA 28.2NA 27.6NA 27.9NA	34,8NA 35,2NA 34,8NA 34,3NA	30,3NA 29,9NA 30,0NA 29,5NA		
ILDP	1.0001					•
IL1 IL2 IL3 IL4	-20,0UA -20,0UA -5,00UA					

PASSED GALPAT (WIDE LIMITS) VCC=1AV PASSED GALPAT (TIGHT LIMITS) VCC=1AV PASSED GALPAT (TIGHT LIMITS) VCC=5V

	vec	= 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA) (TDS) (TDH)	26,0N 26,0N	20.0N 20.0N 20.0N	65.0N 8.70N 10.0N
ADDRESS SETUP TIME ADDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WIDTH	(TAS1) (TAS2) (TAH) (TWP)	16.0N 128.N -18.0N 76.0N	14.0N 104.N -14.0N 64.0N	4.00N 46.0N +4.00N 34.0N
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS1) (TCSS2) (TCSH1) (TCSH2)	168.N 166.N 36.0N 49.0N	142 N 142 N 32 M 34 M 34 M	70,0H 68,0N 22,0N 28.0N
OUTPUT ACTIVE FROM CS OUTPUT ACTIVE FROM CS OUTPUT ACTIVE FROM MR	(SADOT) S	264.N 262.N 50.0N	216.1 212.1 44.00	90,0N 90,0N 26.0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH1) (TDOH3) (TDOH3) (TPOH) (TRC) (TWC)	146.N 140.N 138.N 134.N 272.N 248.N	112,N 108,N 116,N 110,N 224,N	30,0N 30,0N 34,0N 32.0N 120.N 120.N
IIL	IIH	VICI	VICS	
	200.PA 300.PA 200.PA 200.PA	3.01 V 3.06 V 3.07 V 3.05 V	-2.99 V -3.09 V -3.09 V -3.10 V	
A4 =200.PA A5 =300.PA A6 =300.PA A7 =300.PA	200,PA 300,PA 200,PA 300,PA	3.09 V 3.00 V 3.02 V	-3,10 V -3,03 V -3,04 V -3,02 V	·
CS1 =200.PA CS2 =300.PA MWR =300.PA MRD =300.PA	300.PA 200.PA 200.PA 400.PA	3.02 V 3.05 V 3.02 V 3.01 V	-3,03 V -3,07 V -3,06 V -3,08 V	
DIO -500.PA DI1 -300.PA DI2 -300.PA DI3 -300.PA	200.PA 200.PA 200.PA 300.PA	3.11 V 3.11 V 3.11 V 3.08 V	+3,05 V +3,04 V +3,05 V +3,05 V	

RCA	CDP1822\$D	256 X 4 CMOS	STATIC RAM	31 AUG 78	ŤEMP:	#20 C	sn:	7
					PAGE	4 OF	10	
	מסמ	DO1	pož	003				

	ทอด	001	Doa	003
VOL1 VOL2 VOH1 VOH2	105.MV 100.MV 4.86 V 9.80 V	105 MV 110 MV 4,87 V 9,81 V	110 MV 125 MV 4 86 V 9 80 V	110, MV 115. MV 4,86 V 9.81 V
IDN1 IDN2 IDP1 IDP2	7.15MA 18.4MA -2.85MA -6.31MA	6.85MA 17.0MA -2.88MA -6.41MA	6.60MA 15.5MA 42.85MA 48.21MA	6.75MA 16.0MA 72,91MA #6.48MA
1071 1072 1023 1024	7.60NA 4.20NA 4.50NA 8.20NA	1,2MNA 3,8MNA 4,5MNA 1,2MNA	7,70NA 4,90NA 3,00NA 6,60NA	700.PA 2.70NA 5.20NA 1.90NA
1025 1026 1027 1028	2.00NA 2.10NA 2.00NA 1.80NA	6.00NA 6,40NA 6,10NA 6.60NA	2.40NA 2.40NA 2.30NA 2.40NA	5.50NA 5.50NA 5.50NA
ILDP	⊷200.NA			
IL1 IL2 IL3 IL4	-20.0UA -20.0UA -5.00UA -5.00UA			

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÷			C=10V		
•	PASSED GALPAT (TIGHT PASSED GALPAT (TIGHT		C=5V	REPRODUCII ORIGINAL P	BILITY OF THE AGE IS POOR
	PASSED DATA RETENTION	TEST			MOOJ OF GETT
٠.		van	* 4.5V	5'.ØV	10,0V
	ADDRESS ACCESS TIME	(TAA)	280 a N	215.N	ва, ом
•	DATA SETUP TIME	(TDS)	30.0N	85.9V	8.00N
	DATA HOLD TIME	(нат)	8.00N	8,000	10.0N
	ADDRESS SETUP TIME	(TAS1)	14.0N	10.0N	4.7 N
	ADDRESS SETUP TIME	(TAS2)	139.N	100 N	42.0N
	ADDRESS HOLD TIME	(YAH)	-18,0N	= 14 . AN	#4. PON
	WRITE PULSE WINTH	(TWP)	84 . ØN	70.0N	32.0N
	CS1 SETUP TIME	(TUSSS)	168.N	134°N	64, DN
	CS2 SETUP TIME	(TOSSE)	168.N	134.N	65 an
•	CS1 HOLD TIME	(TCSH1)	48,0N	38.0N	50,0N
	CS2 HOLD TIME	(TCSH2)	50.0N	38.ª ØN	20.0N
	OUTPUT ACTIVE FROM CS	31 (TOOA1)	272.N	210, N	88 ៧៧
	OUTPUT ACTIVE FROM CS		268.N	210.N	88, QN
	OUTPUT ACTIVE FROM ME		48.ØN	42.0N	24.0N
	OUTPUT HOLD FROM CS1	(TDOH1)	138.N	106 N	26, 8N
	OUTPUT HOLD FROM CS2	(SHOOT)	134.N	1 45 ° N	26, ØN
	OUTPUT HOLD FROM MRD	(EHOOT)	136.N	114,N	30,0N
	ООТРОТ НОСО ЕРОМ МИК	(TPDH)	134.N	110 N 208 N	32.0N
	READ CYCLE TIME	(TRC)	248 N	208,N	112.N
	WRITE CYCLE TIME	(TWC)	224.N	200'N	96. BN
	IIL.	11H	VIC1	VTCR	
	A 00,00 A	190,PA	3_10 V	-3,08 V	
•	A1 -100.PA	100 PA	3.15 V	-3,16 V	
	A2 0.00 A	100,PA	3.15 V	43,17 V	
	A3 =100.PA	100.PA	3.14 V	#3.18 V	
	A4 0.00 A	100,PA	3.17 V	+3' 17 V	
	A5 =100.PA	100.PA	3,09 V	-3,12 V	
	A6 -100.PA	100,PA	3,11 V	-3,13 V	
	A7 =100.PA	100.PA	3.11 V	#3_11 V	
	CS1 -100.PA	100, PA	3 . 11 V	-3,12 V	
	CS2 -100,PA	100.PA	3.13 V	-3,14 V	
<i>/</i> .	MWR =100.PA	IMM,PA	3,11 V	+3,14 V	
	MRD =100.PA	100.PA	3.11 V	#3.10 V	
	DIO -100.PA	1 M C . P A	3.19 V	-3,14 V	
	DI1 0.00 A	100,PA	3.19 V	-3,13 V	
	DI2 ~100.PA	100,PA	3.18 V	=3,13 V	
	DI3 0.00 A	100.PA	3.16 V	-3,13 V	
			B-65		
-					

RCA	CDP1822SD	256 X 4	CHOS STATIC RAM	31 AUG 78 TE	MP: +55	C SNI	7
				p	Age 6	Of 10	

	poa	100	200	003
VOL1	95.0MV 90.0MV	100 MV	100,MV	100 MV
VOLE	4.88 V	100.MV 4,88 V	110,MV 4,88 V	105.MV 4.89 V
ADHS	9.84 V	9_84 V	9,84 V	9 84 V
IDN1	7.85MA	7.50MA	7'25MA	7,35MA
IDN2	20,5MA	19.0MA	17.4MA	17.9MA
IDPi	-3.25MA	∞3,37MA	#3.30MA	-3.35MA
IDP2	-7.23MA	-7-44MA	#7.19MA	-7.49MA
IOZi	4,60NA	200.PA	2.40NA	800 PA
1015	5,50NA	-1,90NA	5,20NA	-1,8MNA
1023	#1.50NA	5,10NA	-1.80NA	5,30NA
1024	300.PA	3 1 0 NA	#900 PA	ANOB.E
1025	3,70NA	-1.10NA	4.10NA	-1,80NA
1026	3,80NA	-1.20NA	3.90NA	-1,60NA
1077	3.70NA	-900 PA	4,00NA	#1.80NA
1078	3.70NA	-1.20NA	3.80NA	-1.70NA

ILDP -15'. 0UA

IL1 #15,0UA IL2 =15,0UA IL3 #5,00UA IL4 #5,00UA

RCA	CDP1822SD	256 X 4	CMOS STATIC RAM	31 AUG 78	TEMP	85 C	SN:
			· · · · · · · · · · · · · · · · · · ·		· -: •		

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PASSED	GALPAT	(WIDE	LIMITS)	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS	VCC=10V
PASSED	GALPAT	CTIGHT	LIMITS)	VCC=5V

CHICANAMI, PAGE: 155 HOOR

	vcc	# 4.5V	5. 0V	10.0V
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA) (TDS) (TDH)	280.N 24.0N 14.0N	235'N 20.0N 14.0N	107.N 8.70N 14.0N
ADDRESS SETUP TIME ADDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WIDTH	(TAS1) (TAS2) (TAH) (TWP)	8.00N 134.N -20.0N 84.0N	8.00N 114.N -16.0N 74.0N	42.0h 58.0n -6.00n 4.00n
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS1) (TCSS2) (TCSH1) (TCSH2)	186.N 182.N 50.ON 54.ON	162 N 158 N 46 ON 48 ON	84, 20 82, 20 88, 20 88, 20 88, 20
OUTPUT ACTIVE FROM CS1 OUTPUT ACTIVE FROM CS2 OUTPUT ACTIVE FROM MRO	(YDOA1) (SAOUT) (EAOUT)	272.N 268.N 60.0N	232, N 230. N 54. MN	112.N 117.N 30.0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH1) (TDOH2) (TDOH3) (TPOH) (TRC) (TWC)	158.N 154.N 140.N 140.N 304.N 248.N	126, N 122, N 120, N 116, N 256, N 224, N	40°0N 40°0N 38°0N 40°0N 136°N
IIL IIH	I	VIC1	vica	
A1 ~18,4NA 19. A2 ~17,8NA 18.	ANA BNA ANA 4NA	2.89 V 2.95 V 2.96 V 2.94 V	#2,88 V #2,97 V #2,98 V #2,99 V	
A5 =18.8NA 19. A6 =18.8NA 18.	1NA 3NA 2NA BNA	2.98 V 2.89 V 2.91 V 2.91 V	-2.99 V -2.91 V -2.93 V	
CS2 #19.0NA 18. MWR #18.5NA 17.	9NA 4NA 9NA 5NA	2.91 V 2.93 V 2.90 V 2.90 V	=2,91 V =2,97 V =2,95 V =2,91 V	
DI1 =18.1NA 17. DI2 =17.6NA 18.	1 N A 7 N A 4 N A 8 N A	3.00 V 2.98 V 2.98 V 2.96 V	*5'64 A *5'64 A *5'64 A	

RCA	CDP1822SD	256 X 4 CHOS	STATIC RAM	31 AUG 78	TEMP	85 C	SN:
					PAGE	8 OF	10
	DOG	001	soa	DOZ		•	
VOH2 VOH1 VOH1	135.MV 140.MV 4.80 V 9.72 V	140,MV 150.MV 4,81 V 9,72 V	150.MV 170.MV 4.80 V 9.72 V	145 MV 160 MV 4 80 V 9 73 V	·		
1005 1001 1001	5.50MA 13.6MA -2.02MA -4.50MA	5.25MA 12.6MA ~2,05MA -4.55MA	5.05MA 11.4MA 2.00MA 24.41MA	5,15MA 11.8MA #2,06MA #4.62MA			
1021 1022 1023 1024	313.NA 301.NA 305.NA 299.NA	300', NA 304', NA 302', NA 299', NA	321,NA 321,NA 320,NA 323,NA	AN , CEE AN , WEE AN , CEE AN , 65E			
1025 1026 1027 1028	303, NA 312, NA 313, NA 303, NA	307,NA 297,NA 304,NA 305.NA	328.NA 339.NA 325.NA 327.NA	339, NA 328, NA 340, NA 328, NA			
ILDP	15°,0UA						
IL1 IL2 IL3 IL4	#35,0UA #35,0UA #20,0UA #15,0UA						

PASSED DATA RETENTION TEST

	vcc	= 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	290 N	245'N	110.0
DATA SETUP TIME	(TDS)	24.ØN	28.QN	10,0N
DATA HOLD TIME	(TDH)	16.0N	16.0N	14 . DA
DATA 110E0 1111E	(, any	7. Cl = \$1.44		1 7 4 60.
ADDRESS SETUP TIME	(TAS1)	4.00N	4. ดุดุก	4.00N
ADDRESS SETUP TIME	(TAS2)	136.N	122.N	66. NN
ADDRESS HOLD TIME	(TAH)	-20,0N	=18.0N	#6,00N
WRITE PULSE WIDTH	(TWP)	92.00	82.0N	46.0N
CS1 SETUP TIME	(TCSS1)	198,4	172 N	92 2N 88 0N
			1 / G p 14 4 7 / M	9 E 9 E 14
CS2 SFTUP TIME	(TCSS2)	194.N	170.N	70 00
CS1 HOLD TIME	(TCSH1)	54,0N	48. ON	30,01
CS2 HOLD TIME	(TCSH2)	60.0N	52.0N	30 ON
OUTPUT ACTIVE FROM CS	(TDOAT)	288,N	248, N	126.N
DUTPUT ACTIVE FROM CS	(SAOOT) SE	284 N	246 N	122.N
DUTPUT ACTIVE FROM MR		64.0N	58.9N	34. ØN
DUTOUT WALL TOOM CC.	(\tag{\tag{\tag{1}}}	148 N	130°N	44, ØN
OUTPUT HOLD FROM CS1	(TDOH1)	160.N		electric to the electric to
OUTPUT HOLD FROM CS2	(SHOOT)	156.N	126,N	42, ØN
OUTPUT HOLD FROM MRD	(TDOH3)	142,N	150°N	38, ØN
OUTPUT HOLD FROM MWR	(ፕΡባዘ)	142.N	118 N	40.0N
READ CYCLE TIME	(TRC)	312.N	272,N	144.N
WRITE CYCLE TIME	(TWC)	256 _m N	232.N	144 . N
IIL	IIH	vici	VICE	
AØ =107,NA	109,NA	2.88 V	=2,86 V =2,95 V	
A1 -107.NA	109 NA	2.94 V	-2 05 V	
A2 -107,NA	107.NA	2.95 V		
			=2,97 V	
A3 #108.NA	107.NA	2.93 V	-2.98 V	
A4 -104,NA	101.NA	2.97 V	÷2,98 V	
A5 -108,NA	107.NA	2,87 V	#2,89 V	
A6 . #106_NA	103,14	2.89 V	÷2,91 V	
A7 -106.NA	103.NA	2.89 V	-2.89 V	
CS1 =109.NA	103,NA	2 00 4	=2,90 V	
		2.89 V	™⊆ _₽ 70 V _3 04 U	
CS2 =104.NA	103.NA	2.92 V	±5°4€ ∧	
MHR #108.NA	103,NA	2.89 V	#2,94 V	
MRD -104,NA	105.NA	8.88 V	-5.40 A	
DIØ -105.NA	102.NA	2.98 V	-2,93 V	
DI1 -104.NA	101 NA	2.97 V	45,45 A	
DI2 #99,5NA	101.NA	2.97 V	-2,93 V	
DI3 #101.NA	98.3NA	2,95 V	#2.93 V	
MANA MERICANA	AUE BIAM	C°23 A	™¢°23 \	

RÇA	CDP1822SD	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP
	. •				PAGE
	non	001	500	003	
AOH AOF AOF	2 155.My 1 4.78 v	160, MV 170, MV 4, 78 V 9, 69 V	165.MV 190.MV 4.78 V 9.68 V	160° MV 180° MV 4° 78 V 9° 69 V	
ION ION IOP IOP	2 12.2MA 1 =1,81MA	4.70MA 11.2MA -1.84MA -4.08MA	4.50MA 10.1MA #1.80MA #3.96MA	4.65MA 10.5MA 91.86MA 94.15MA	
10Z 10Z 10Z 10Z	2 1,28UA 3 1,30UA	1,25UA 1,26UA 1,25UA 1,25UA	1,38UA 1,36UA 1,38UA 1,36UA	1,38UA 1,39UA 1,38UA 1,39UA	
102: 102: 102:	6 1.31UA 7 1.30UA	1,26UA 1,26UA 1,26UA 1,26UA	1.40UA 1.39UA 1.38UA 1.37UA	1 41 U A 1 40 U A 1 40 U A 1 40 U A	
rld.	AUQ.OS 9				
IL1 IL2 IL3	#90.0UA #105.UA #80.0UA				

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10 OF 10

SN:

PAGE 1 PF 10

PASSED GALPAT	(WIDE LIMITS) (TIGHT LIMITS)	VCC×1ØV	REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR
PASSED GALPAT	(TIGHT LIMITS)	VCC=5V	CTATOWN IN

1,1				
	yer	; = 4.5V	5. PV	10.0V
ADDRESS ACCESS TIME	(TAA)	285.N	205"N	75.0N
DATA SETUP TIME	(Tps)	24,0N	18.0N	8.00N
DATA HOLD TIME	(TDH)	10.0N	10.0N	10 ØN
	(1,511,5		# *: # *!!!	10.0
ADDRESS SETUP TIME	(TAS1)	14.0N	12.00	4.00N
ADDRESS SETUP TIME	(TAS2)	130 N	106.N	48.ØN
ADDRESS HOLD TIME	(HAT)	-22,0N	-18.0N	-4.00N
WRITE PULSE WINTH	(TWP)	74.0N	66.AN	36.0N
CS1 SETUP TIME	(70881)	170.N	144 N	. ค่า เกา
CS2 SETUP TIME	(TCSS2)			68, ØN
		166.N	142.N	66.0N
	(TCSH1)	38,0N	34.0N	ea, øn
CSS HOLD TIME	(TCSH2)	42.ØN	36.0N	55.0N
OUTPUT ACTIVE FROM C	S1 (TDOA1)	366*N	218'N	94 , ØN
OUTPUT ACTIVE FROM C		P64.N	216.N	90,0N
OUTPUT ACTIVE FROM M		54.0N	48. ØN	26. NN
		70 -3 M 2014		
OUTPUT HOLD FROM CS1	(TDOH1)	154,N	122,N	38, ØN
OUTPUT HOLD FROM CS2	(SHOUT)	150 N	120,N	38, ØN
OUTPUT HOLD FROM MRD		142.N	120,0	30,0N
OUTPUT HOLD FROM MWR	=	142.N	116.N	32.0N
READ CYCLE TIME	(TRC)	280 N	2.62	
WRITE CYCLE TIME	(TWG)		232, N	120.N
MARIE GINEC ITHE	(W.L.)	256.N	192.N	112.N
TIL	IIH	VICI	Alcs	
A00 -1.90NA	1.70NA	2.99 V	-2,98 V	
A1 =1.60NA	1,70NA			
A2 -1.60NA		3,91 V	≈3,03 V	
	1.80NA	3.05 V	-3,09 V	
A3 +1.70NA	1.50NA	3.04 V	-3'.07 V	
A4 #1.80NA	1,90NA	3_94 V	-3 08 V	
A5 #1,80NA	1,90NA	2.99 V	-3,03 V	
A6 -1.50NA	AND8,S	3.01 V	-3 05 V	
A7 =2,00NA	2.40NA	3.01 V	+3,05 V +3,03 V	
CS1 -1.90NA	1,90NA	3_04 V	-3,04 V	
CS2 -1,80NA	1,80NA	3.06 V	-3,09 V	
MWR -1,60NA	1,70NA	2,98 V	-2,99 V	
MRD #2.10NA	2.20NA	3,90 V	-3.01 V	
DIØ #2.10NA	2.40NA	3.13 V	-3.08 V -3.06 V -3.09 V	
DI1 -2.18NA	1,90NA		25 WY A	
		3.12 V	ע ממיקבי	
	2.20NA	3.12 V	+5,09 V	
DI3 =1,90NA	2.10NA	3.11 V	-3.07 V	

RCA	CDP1822SD	256 X 4 CMDS	STATIC RAM	31 AUG 78	TEMP:	25 C SN:	8
					PAGE	2 OF 10	
	, ממס	001	poz	003			
AOH5 AOH1 AOT5 AOT1	120.MV 115.MV 4.84 V 9.78 V	125.MV 130.MV 4.84 V 9.78 V	130.MV 145.MV 4.84 V 9.77 V	125, MV 140, MV 4,84 V 9,78 V			
ION1 ION1 IOP1 IOP2	6.15MA 16.1MA -2.47MA -5.59MA	5.95MA 14.8MA -2.45MA -5.57MA	5.60MA 13.0MA =2.43MA =5.43MA	5,80MA 13,6MA 2,50MA 5,72MA			
1021 1022 1023 1024	32,0NA 28,2NA 24,6NA 27,6NA	15,7NA 16,8NA 20,7NA 17,6NA	58,5NA 57,0NA 52,5NA 53.8NA	16,9NA 16,5NA 22.3NA 20.0NA			
1025 1026 1027 1028	26,2NA 26,8NA 27,3NA 26,5NA	17.8NA 18.0NA 17.5NA 18.0NA	54,1NA 55,5NA 55,3NA 58.6NA	18,6NA 18,0NA 18,1NA 17.7NA			
ILDP	⇔5,00UA						
IL1 IL2 IL3 IL4	-15,0UA -15,0UA -65,0UA -50,0UA						

PASSED	GALPAT	(WIDE	LIMITS)	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS	VCC=5V

	vcc	= 4.5V	5.0V	10.00
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA) (TDS) (TDH)	8.00N 88.0N 595.N	8.00N 8.00N 8.00 8.00	80'.0N 8.00N 10.0N
ADDRESS SETUP TIME ADDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WIDTH	(TAS1) (TAS2) (TAH) (TWP)	18.0N 130.N -22.0N 78.0N	14.7N 174.N ~18.7N 60.7N	42.00 42.00 *2.00 *2.00 *2.00
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS1) (TCSS2) (TCSH1) (TCSH2)	170 N 166 N 44 ON 46 ON	142, N 138, N 36, AN 38, AN	52,0N 62,0N 62,0N
OUTPUT ACTIVE FROM CS1 OUTPUT ACTIVE FROM CS2 OUTPUT ACTIVE FROM MRD	(TDDA1) (SADDT) (EADDT)	276.N 274.N 50.0N	216'N 214'N 44.0N	86,0N 82,0N 24.0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR OUTPUT HOLD FROM MWR READ CYCLE TIME	(TDOH1) (TDOH2) (TDOH3) (TPOH) (TRC)	148.N 144.N 140.N 138.N 264.N	114, N 112, N 118, N 114, N 216, N	34,0N 34,0N 30,0N 30,0N 112.N
WRITE CYCLE TIME IIL I	(TWC) Ih	272.N VIC1	VICS Sug'N	96.0N
A1 ≈300.PA 30 A2 ≈300.PA 30	20.PA 70.PA 70.PA 70.PA	3.10 V 3.12 V 3.15 V 3.14 V	3609 V 3613 V 3618 V 3617 V	
A5 -300.PA 30 A6 -300.PA 50	70 PA 20 PA 30 PA 70 PA	3.14 V 3.10 V 3.11 V 3.12 V	=3,18 V =3,13 V =3,15 V =3,13 V	
CS2 #400.PA 30 MWR #300.PA 30	70.PA 70.PA 70.PA 70.PA	3.14 V 3.16 V 3.09 V 3.11 V	#3,14 V #3,18 V #3,11 V	
DI1 +500.PA 40	70.PA 70.PA 70.PA 20.PA	3.23 V 3.21 V 3.21 V 3.20 V	-3,17 V -3,16 V -3,17 V -3,16 V	

RCA	COP182250	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP	ASQ C	SNI
					PAGE	4 OF	10
	non	DO1	DOS	003			
VOL 1	110.MV	110, MV	115.MV	115, MV			
VOLE		115.MV	125.HV	120°. MV 4,87 V 9.82 V			
VOH1		4,87 V	4,86 V	4,87 V			
VOHS	9 82 V	9.81 V	9.80 V	9.82 V			
ION1	6.75MA	6,55MA	6.25MA 15.0MA	6 # 40MA			
IDNS	18,3MA	16.8MA	15.0MA	15.5MA			
IDP1	F2.89MA	-2.88MA	⇒2 _≠ 55MA	#2,94MA			
1065	⇔6.5 8MA	-6.57MA	⇔6.4ØMA	19.5MA 22,94MA 46.73MA			
IOZI	9,90NA	2.40NA	25, 1NA	3 29NA			
IOZZ	10.7NA	500.PA	33,2NA	500 PA			
1023	4.00NA	7.70NA	26,9NA 27,0NA	7,40NA 6,00NA			
10Z4	6.10NA	5.50NA	27.0NA	P. BONY			
1029	9.20NA	1,10NA	ANS SE	800 PA			
1026		1,30NA	31,0NA	500 PA			
IOZ7		1,00NA	33,4NA	600, PA			
1028	9.30NA	1.10NA	33,4NA 30,7NA	500; PA			
ILDP	□ 15.0UA						
~ ~ ~ .							
ILi	-15,0UA						
ILS	#10.0UA						
IL3	#50,0UA						
IL4	#40.0UA						

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			PAGE	5 OF 10
	IT LIMITS)	/CC=10V /CC=10V /CC=5V	REPRODUCIBILITY ORIGINAL PAGE 1	OF THE S POOR
PASSED DATA RETENTIO	N TEST			
	vo	CC = 4.5V	5.0V	10'.0V
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA) (TOS) (TDH)	295.N 34.0N 6.00N	215'.N 24.0N 6'.00N	70'.0N 8.00N 8.00N
AUDRESS SETUP TIME AUDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WIDTH	(TAS1) (TAS2) (TAH) (TWP)	14.0N 130.N -24.0N 88.0N	10.0N 102.N 18.0N 72.0N	4.00 8.00 -3.00 92.00
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS1) (TCSS2) (TCSH1) (TCSH2)	158.N 54.0N	138, N 134, N 42, ON 44, ON	6(0N 52 0N 28 0N 20 0N
OUTPUT ACTIVE FROM COUTPUT ACTIVE FROM COUTPUT ACTIVE FROM M	(SAOOT) SE	298 ู้พ	214, N 212, N 42.0N	55,0N 80,0N 80,0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TOOH2) (TDOH3)	140 N	110, N 108, N 116, N 112, N 208, N 192, N	54.0N 54.0N 68.0N 28.0N 104.0N
TIL	IIH	VIC1	AICS	
A0 #100.PA A1 #100.PA A2 #100.PA A3 #100.PA	100.PA 100.PA 100.PA 100.PA	3.20 V 3.22 V 3.25 V 3.25 V	-3,19 V -3,24 V -3,29 V -3,27 V	
A4 -100,PA A5 -500,PA A6 -100,PA A7 -100,PA	100.PA 100,PA 200,PA 100.PA	3.24 V 3.20 V 3.21 V 3.21 V	+3,28 V +3,23 V +3,25 V +3,24 V	
CS1 =100.PA CS2 =100.PA MWR =100.PA MRD =200.PA	100,PA 100,PA 100,PA 100,PA	3,25 V 3,26 V 3,20 V 3,21 V	+3,25 V +3,24 V +3,21 V +3,21 V	
DIO =100.PA DI1 =100.PA DI2 =200.PA DI3 =100.PA	100.PA 100.PA 100.PA 100.PA	3.34 V 3.31 V 3.31 V 3.30 V	+3,28 V +3,26 V +3,27 V +3,25 V	
		77 77 7		

RCA	CDP18228D	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP:	₩55 C	s
					PÄGE	6 OF	10
	DOØ	DOI	Soo	003			
VOL1 VOH1 VOH2	4,88 9 9,84 V	105, MV 100, MV 4,88 V 9,84 V	110.MV 115.MV 4.88 V 9.84 V	105' MV 110' MV 4' 88 V 9' 84 V			
ION1 IDN2 IOP1 IOP2	7,30MA 20,0MA =3,32MA =7,54MA	7' 10MA 18 6MA +3 33MA +7 58MA	6.75MA 16.6MA =3.27MA =7.35MA	6.90MA 17.3MA =3.40MA =7.76MA			
10Z1 10Z2 10Z3 10Z4	800.PA 3.30NA 3.60NA -100.PA	5,20NA 2,00NA 1,10NA 4,90NA	16,6NA 20,2NA 24,6NA 18.0NA	5,40NA 2,90NA 300.PA 3,40NA			
1025 1026 1027 1028	6.10NA 6.00NA 6.20NA 6.20NA	=300.PA =400.PA =400.PA =600.PA	20',9NA 18,7NA 18,5NA 18,9NA	200,PA 200,PA -100,PA			
ILDP	⇔5 _a 00UA						
IL1 IL2 IL3 IL4	=10,0UA =10,0UA =45,0UA =35,0UA						

SNI

RCA CDP1822SD 256	X 4 CMOS	STATIC RAM 3	1 AUG 78 TEMP:	85 C SNI	8
			PAGE	7 DF 10	
PASSED GALPAT (TIGH	LIMITS) T LIMITS) T LIMITS)				
PASSED DATA RETENTIO	N TEST				
		vcc = 4.5V	5,0V	10.0V	
LUBBECO LOCECO TEUR	f T a L	1 970 N	225 N	o ธ์หม	

	VCC	= 4,5V	5.0V	10.0V
AUDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA) (TOS) (TOH)	270.N 24.0N 12.0N	225.N 20.0N 12.0N	95.0N 8.00N 12.0N
ADDRESS SETUP TIME ADDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WINTH	(TAS1) (TAS2) (TAH) (TWP)	A . 00 N 130 . N - 20 . 0 N 84 . 0 N	8.00N 106.N -18.0N 72.0N	4.70N 54.0N -4.70N 40.0N
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS1) (TCSS2) (TCSH1) (TCSH2)	178.N 172.N 52.ØN 54.ØN	150°N 148°N 46°QN 48°QN	74,0N 72,0N 26,0N 26,0N
OUTPUT ACTIVE FROM CS1 OUTPUT ACTIVE FROM CS2 OUTPUT ACTIVE FROM MRO	(TODA1) (SADDT)	758.N 256.N 58.0N	24 ° WN 518 ° W 550 ° W	104.N 107.N 28.0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH1) (TDOH2) (TDOH3) (TPDH) (TRC) (TWC)	158.N 154.N 142.N 142.N 288.N 232.N	126, N 124, N 120, N 116, N 248, N 200, N	42,0N 42,0N 34,0N 34.0N 120.N
TIL I	EH	VIC1	VICE	
A1 +19,3NA 20 A2 +19,6NA 20	AN8.0 AN2.0 AN3.0 AN2.0	2.93 V 2.95 V 2.99 V 2.97 V	-2,92 V -3,02 V -3,00 V	
A5 =21,3NA 20	0,9NA 1.0NA 1.5NA 2.8NA	2,97 V 2,93 V 2,95 V 2,95 V	-3,01 V -2,96 V -2,99 V -2,97 V	
CS2 =19,5NA 2: MWR =18,7NA 1:	L.9NA L.5NA 9.8NA 9.2NA	2.98 V 3.00 V 2.91 V 2.94 V	#2,98 V #2,93 V #2,94 V	
DI1 #21,0NA 23 DI2 #21,9NA 23	4.7NA 2.4NA 3.1NA 2.0NA	3.08 V 3.05 V 3.05 V 3.04 V	-3,02 V -3,00 V -3,02 V -3,01 V	

RCA	CDF18225D	256 X 4 CMOS	STATIC RAM	31 AUG 78 TEM	PÍ 85 C SNÍ
				PA	GE 8 OF 10
	DOØ	100	soa	DO3	
AOH 5 AOH 7 AOT 5 AOT 7	135.MV 140.MV 4.81 V 9.73 V	140', MV 150', MV 4', 80 V 9.73 V	150.MV 170.MV 4,80 V 9.72 V	145 MV 165 MV 4.82 V 9.74 V	
ION1 ION2 IOP1 IOP2	5.40MA 13.8MA -2.10MA -4.74MA	5.20MA 12.6MA -2.08MA -4.72MA	4.90MA 11.2MA ⇒2.04MA ⇒4.53MA	5,05MA 11,6MA +2,12MA +4.85MA	
1021 1022 1023 1024	158.NA 161.NA 154.NA 157.NA	148, NA 142, NA 141, NA 145. NA	AM.DES AM.1ES AM.EES AM.TSS	157, NA 160, NA 158, NA 166, NA	
1025 1026 1027 1028	161,NA 151,NA 151,NA 155,NA	145 NA 157, NA 144, NA 146. NA	225.NA 221.NA 225.NA 221.NA	164, NA 165, NA 156, NA 167, NA	
ILDP	6.80UA				
IL1 IL2 IL3 IL4	#35,0UA #40,0UA #85,0UA #70,0UA				

PAGE 9 DF 10

PASSED GALPAT (WIDE L PASSED GALPAT (TIGHT L PASSED GALPAT (TIGHT L	IMITS) VCC=10V	REPRODUCIB ORIGINAL PA	LITY OF THE AGE IS POOR
PASSED DATA RETENTION T	EST		
	VCC = 4.	5V 5.0V	10:0V
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TDS) 24	0.N 230.N .0N 20.0N .0N 12.0N	100.N 8,00N 14.0N
ADDRESS SETUP TIME ADDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WIDTH	(SRAT) 13 (SR= (HAT)	00N 6.00N 2.N 112.N .0N -18.0N .0N 78.0N	4.00N 60.0N -6.00N 44.0N
CS: SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS2) 17 (TCSH1) 54	2.N 158,N 8.N 154.N .ON 48.GN	82,0N 78,0N 30,0N 28.0N
OUTPUT ACTIVE FROM CS1 OUTPUT ACTIVE FROM CS2 OUTPUT ACTIVE FROM MRD	(SA00T)	0.N 234.N 6.N 230.N .ON 54.0N	114.N 112.N 30.0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM CS2 OUTPUT HOLD FROM MWR OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH2) 15 (TDOH3) 14 (TPDH) 14 (TRC) 29	8.N 128.N 6.N 124.N 2.N 122.N 4.N 118.N 6.N 256.N	44,0N 44,0N 36,0N 38.0N 128.N 136.N
TII. III	vict	VECS	
A1 -116.NA 120 A2 -117.NA 119 A3 -115.NA 119	3.NA 2.89 3.NA 2.92 3.NA 2.96 5.NA 2.94	V =2,94 V V =3,00 V V =2,97 V	
A5 #120.NA 119 A6 #113.NA 120	3.NA 2.94 9.NA 2.90 1.NA 2.93	V #2,93 V V #2,96 V	

2.95 V

2.97 V

V 88.5

3.05 V

3.02 V 3.02 V -2,94 V

-3.00 V -2.89 V -2.91 V

-2.99 V

-2.97 V -3.00 V -2.98 V

CS1

csa

MWR

MRD

DIO

DII

015

DI3

-118.NA

-114.NA

-113.NA

=119,NA

-116.NA

-118,NA

#116.NA

-113,NA

AN,151 AN,151

114,NA

120.NA

126.NA

119,NA

118,NA

117 NA

RCA	CDP18225D	256 X 4	CHOS STATIC	RÅM 31	AUG 78	TEMPİ	125 C	eni	8
						PAGE	15 05 1	Ŕ	

	DOØ	001	bos	003
AOHS	150 MV	155 MV	170.MV	165 MV
AOH!	155 MV	170 MV	195.MV	185 MV
AOFS	4 79 V	4,79 V	4.78 V	4,79 V
AOF!	9 70 V	9,70 V	9.69 V	9,71 V
IDN1	4 85MA	4.70MA	4,40MA	4.55MA
IDN2	12 3MA	11.3MA	9,95MA	10.4MA
IDP1	*1 88MA	-1.88MA	=1,85MA	+1.92MA
IDP2	*4 24MA	-4.23MA	+4,09MA	+4.33MA
IOZ1	484.NA	550,NA	646 NA	601, NA
IOZ2	467.NA	539,NA	650 NA	590, NA
IOZ3	464.NA	539,NA	645 NA	589, NA
IOZ4	465.NA	531,NA	654 NA	582. NA
1025	469.NA	542,NA	658 NA	600, NĀ
1026	477.NA	531,NA	659 NA	596, NĀ
1027	469.NA	540,NA	645 NA	599, NA
1028	460.NA	535,NA	662 NA	588. NA
ILDP	40'. QUA			

ILDP 40.0UA
IL1 *95.0UA
IL2 +115.UA
IL3 +150.UA
IL4 +125.UA

				PÄGI	1 OF 10
PASSED	GALPAT (TIGH	T LIMITS) VI	CC=10V CC=10V CC=5V	REPRODUCIBII ORIGINAL PAG	TY OF THE
PASSED	DATA RETENTIO	N TEST			
		VC	2 = 4.5V	5.øv	10,0V
ADDRES	S ACCESS TIME	(TAA)	530.N	195.N	85.0N
	ETUP TIME	(TDS)	24.0N	20.0N	8.00N
DALA M	OLD TIME	(TDH)	10.0N	10.5N	10.0N
	S SETUP TIME	(TAS1)	12.04	10,0N	4.00N
	S SETUP TIME S HOLD TIME	(SZAT) (HAT)	112.N	94.0N	46.0N
	PULSE WIDTH	(TWP)	-18,0N 66,0N	-14.0N 60.0N	-4.00N 36.0N
C81 5	ETUP TIME	(TCSSI)	158.N	136,N	68,00
	ETUP TIME	(TCSS2)	154.N	130,N	64,0M
	OLD TIME	(TCSH1)	40,0N	36,0N	55,0M
CS2 HI	DLD TIME	(TCSH2)	45. QN	36. ØN	55.0N
OUTPUT	ACTIVE FROM C	S1 (TDGA1)	226 aN	192,N	១៧ ខ្លែស
•		S2 (TDOAZ)	224 N	188 N	90,0N
UUTPUT	ACTIVE FROM M	RD (TDOA3)	50,0N	TT ON	56.0N
	HOLD FROM CS1	(TDOH1)	146.N	1 1 4 N	32,0N
	HOLD FROM CS2		142.N	112 N	32.0N
	HOLD FROM MRD HOLD FROM MWR	(TDOH3) (TOH)	140.N 136.N	116,N 112,N	30.0N 32.0N
	YCLE TIME	(TRC)	248 N	208,N	120 N
WRITE (CYCLE TIME	(TWC)	280 ₈ N	184.N	117.N
	IIL	IIH	VICI	VICR	
0A	-2,60NA	1,60NA	2.81 V	+2,82 V	
ΥĪ	-1.50NA	1.20NA	2.85 V	-2,87 V	
42 43	=1,7UNA =1,80NA	1,50NA 1,60NA	2.88 V 2.87 V	=2,91 V =2,89 V	
~-	- I g d p ii A	1 9 0 0 14 14	C.O. Y		
A 4	•1.9ØNA	1,50NA	2.89 V	+2,93 V	
A5 A6	#1.70NA #1.50NA	1,20NA 1,50NA	2.84 V 2.84 V	=2,87 V =3,87 V	
A7	-1.80NA	1.40NA	5.86 V	#2,87 V #2,88 V	
CS1	_ 4 ///3 N A	4 001514	5 80 W	- •	
C\$5	-1.40NA -1.50NA	1,40NA 1,90NA	2.89 V 2.93 V	€2,89 V €2,93 V	
MWR	-1,80NA	8,10NA	2.84 v	÷2,86 V	
MRD	-1,60NA	1.40NA	2.87 V	-2.86 V	
DIØ	≈1,50NA	1,30NA	2.97 V	±2′,93 V	
DII	-1,50NA	1,30NA	2.94 V	#2,89 V	
DI3 DI2	=2.10NA =2.20NA	1,70NA	2.97 V	=2,91 V	
17.73	ec a cont	1.50NA	2,94 V	⇔2189 V	

RCA	CDP1822SD	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP	25 C
	•		•		PAGE	2 OF
	boø	001	pož	003		
VOL: VOL: VOH:	100.MV 105.MV 4.86 V 9.79 V	105 MV 115 MV 4,86 V 9,79 V	110,MV 130,MV 4,85 V 9,78 V	110, MV 130. MV 4,86 V 9.80 V		
10N1 10N2 10P1 10P2	7.40MA 17.9MA -2.67MA -5.88MA	7.05MA 16.3MA -2.66MA -5.91MA	6.60MA 14.4MA #2.61MA #5.72MA	6,70MA 14,9MA 22,68MA 5,27MA		
1021 1022 1023 1024	18.2NA 19,9NA 22,4NA 19,4NA	25,4NA 23,1NA 19,9NA 22,6NA	19,9NA 20,7NA 25,1NA 22,2NA	26.6NA 24.7NA 19.0NA 22.2NA		
1025 1026 1027 1028	22,2NA 21,8NA 22,0NA 21,3NA	21.5NA 21.7NA 21.9NA 21.6NA	22,7NA 23,0NA 22,5NA 22,6NA	23,3NA 23,4NA 23,5NA		
ILDP	-5,00UA					
IL1 IL2 IL3 IL4	-20,0UA -5,00UA -20,0UA -6,00UA					

SNE

PAGE 3 OF 10

PASSED	GALPAT	(MIDE	LIMITS	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS)	VCC#10V
PASSED	GALPAT	(TIGHT	LIMITS)	VCC=5V

	vcc	= 4.5y	5.øv	10.0V
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA) (TDA) (TDH)	240,N 26.0N 8.00N	195.N 20.70 8.00N	75.4N 8.70N 10.0N
ADDRESS SETUP TIME ADDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WIDTH	(TAS1) (TAS2) (TAH) (TWP)	16.0N 110.N -18.0N 72.0N	12.0N .90.0N -14.0N 58.0N	4.00 42.00 42.00 4.00 32.00
CS1 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS1) (TCSS2) (TCSH1) (TCSH2)	154,N 150,N 38,0N 38,0N	130°N 126°N 38°N 38°N	20,00 22,00 60,00 7,00
OUTPUT ACTIVE FROM CS OUTPUT ACTIVE FROM CS OUTPUT ACTIVE FROM MR	(SAOUT) S	226.N 224.N 46.0N	186° N 184° N 40° ON	86.0N 82.0N 24.0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH1) (TDOH2) (TDOH3) (TPOH) (TRC) (TWC)	138.N 136.N 136.N 132.N 232.N 200.N	106, N 106, N 116, N 110, N 200, N 176, N	30,000 30,000 30,000 312.00 112.00
TIL	IIH	VICi	VICP	
A1 -200.PA A2 =400.PA	200.PA 200.PA 200.PA 200.PA	2.91 V 2.95 V 2.98 V 2.97 V	-2,93 V -2,96 V -3,00 V -2,99 V	
AS =300.PA A6 =200.PA	200.PA 200.PA 200.PA 200.PA	2.99 V 2.94 V 2.94 V 2.96 V	#3.02 V #2.96 V #2.97 V #2.97 V	
CS2 +200.PA MWR +300.PA	200.PA 300.PA 1.70NA 200.PA	2.98 V 3.02 V 2.94 V 2.97 V	-2,98 V -2,95 V -2,95 V	
DI1 =200.PA DI2 =400.PA	200.PA 200.PA 300.PA 200.PA	3.07 V 3.04 V 3.07 V 3.04 V	-3.03 V -3.00 V -3.00 V	

RCA	CDP18225D	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP	#20 C	ន្ទN ខ្
					PAGE	4 OF	10
	poø	001	200	003			
VOL1 VOL2 VOH1	85.0MV 90.0MV 4.88 V	95.0MV 100.MV 4.88 V 9.83 V	100 MV 115 MV 4 88 V	95.0MV 110.MV 4,88 V 9.82 V			
VOH2 IDN1 IDN2 IDP1 IDP2	9.82 V 8.35MA 20.5MA -3.16MA -6.91MA	7,90MA 18,7MA +3,14MA +6,97MA	9.82 V 7.45MA 16.7MA #3.14MA #6.79MA	7,55MA 17,1MA 23,17MA 27,04MA			
1071 1072 1073 1074	3.20NA 600.PA 7.70NA	# 30NA 7 40NA 300 PA 400 PA	4.00NA 900.PA 6.50NA 6.80NA	2,80NA 6,30NA 1,30NA 200,PA		٠.	
1025 1026 1027 1028	500.PA 800.PA 400.PA	6,70NA 6,90NA 6,80NA 7,00NA	500 PA 300 PA 500 PA 200 PA	7, 40NA 7, 10NA 7, 30NA 7, 20NA			
ILDP	=5.00UA						
IL1 IL2 IL3 IL4	-15,0UA -5,00UA -15,0UA -5,00UA						

RCA COPIBEESD P56	X 4 CMOS STA	TIC RAM	31 AUG 78 YEMPI PAGE	±55 C \$N; 5 OF 10
PASSED GALPAT (WIDE PASSED GALPAT (TIGH PASSED GALPAT (TIGH	T LIMITS) VC	:C≈1ØV :C=1ØV :C=5V		
PASSED DATA RETENTIO	N TEST			
	VCC	= 4.5V	5 . Ø V	10,0V
ADDRESS ACCESS TIME	(TAA)	240.N	185' N	70,0N
DATA SETUP TIME	(TDS)	32'.0N	24 on	8.00N
DATA HOLD TIME	(TDH)	6.00N	6 oon	8.00N
ADDRESS SETUP TIME ADDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WINTH	(TAS1)	14.0N	10.0N	35.0N
	(TAS2)	110.N	88,0N	-2.0N
	(TAH)	-18.0N	-14,0N	-3.0N
	(TWP)	64.0N	62.0N	-3.0N
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS1)	152.N	126,N	58,0N
	(TCSS2)	150.N	122,N	56,0N
	(TCSH1)	46.BN	38,MN	22,0N
	(TCSH2)	42.BN	36.MN	18.0N
OUTPUT ACTIVE FROM COUTPUT ACTIVE FROM COUTPUT ACTIVE FROM M	S2 (TDOAR)	230.N 228.N 44.0N	182.N 182.N 38.ØN	55 0 N 80 0 N 82 0 N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH1)	132.N	100 N	22.00
	(TOOH2)	132.N	100 N	28.00
	(TOOH3)	136.N	114 N	28.00
	(TPOH)	132.N	108 N	28.00
	(TRC)	216.N	184 N	104.0
	(TRC)	248.N	176 N	96.0
IIL	IIH	Alci	VTC2	
A0 ==100.PA	100.PA	3.01 V	-3,02 V	
A1 0.00 A	100.PA	3,05 V	-3,06 V	
A2 ==100.PA	0.00 A	3,08 V	-3,10 V	
A3 0.00 A	100.PA	3,08 V	-3,09 V	
A4 =100.PA	0.00 A	3.09 V	#3,12 V	
A5 0.00 A	100.PA	3.03 V	#3,06 V	
A6 =100.PA	100.PA	3.04 V	#3,06 V	
A7 =100.PA	100.PA	3.05 V	#3,06 V	
CS1 = 100.PA	100.PA	3.98 V	-3,08 V	
CS2 = 100.PA	100.PA	3.12 V	-3,12 V	
MWR = 100.PA	400.PA	3.04 V	-3,05 V	
MRD = 100.PA	100.PA	3.06 V	-3,05 V	
DIO 0.00 A	0.00 A	3.16 V	#3,12 V	
DII 0.00 A	0.00 A	3.14 V	#3,08 V	
DIO -100.PA	100,PA	3.16 V	#3,10 V	
DI3 -100.PA	100.PA	3.13 V	#3,08 V	

RÇA	CDP18225D	256	X 4	¢Mos	STATIC	RAM	31	ALIG	78	TEMPÍ	#55 C	SNI	ļ
	•									PAGE	6 OF	10	
	000		gg	1	סס	<u>.</u>		Dt)3				
VOL: VOL: VOH: VOH:	85.0MV 4.89 V		90 4,	.ØMV .ØMV 89 V 85 V	100 4 - 8	.ØMV 1.MV 39 V 34 V		9 0 1 0 4 1	7.0MV 10.MV 89 V 85 V				
ION: ION: IOP: IOP:	22,6MA #3,60MA		20 • 2 ≈	65MA "8MA 64MA 09MA				.1° €3,	25MA 2.1MA 67MA 11MA				
1021 1023 1023	+100.PA 4.00NA		3, -1,	80NA 90NA 20NA 30NA		ONA ONA ONA DNA		-4, -1	50NA 20NA 70NA 60NA				
1025 1026 1027 1028	2.80NA 2.40NA		1 / n :	10na 20na 20na 20na	1 <u>1</u> 2 4 <u>1</u> 5	ANDS SONA SONA SONA		2, 2,	AND, 90NA, 10NA, AND,				
ILDF	° -5,00UA												
IL1 IL2 IL3	=15.0UA =5.00UA =15.0UA						,						

			PAG	SE 7 OF 10
PASSED GALPAT (TIGHT	LIMITS) VO	C=10V C=10V C=5V	REPROD CIBILI ORIGINAL PAGE	
PASSED DATA RETENTION	TEST		•	
	VCC	= 4.5V	5'.0v	10'.0V
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA) (TDS) (TDH)	230.N 24.0N 19.0N	195 <u>'</u> N 20_0N 10_0N	90.0N 8.00N 12.0N
ADDRESS SETUP TIME ADDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WIDTH	(TAS1) (TAS2) (TAH) (TWP)	8.00N 114.N -18.0N 78.0N	8.00N 100.N -14.0N 70.0N	4.00N 52.0N +4.00N 40.0N
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TC\$Si) (TC\$S2) (TC\$H1) (TC\$H2)	164.N 160.N 48.0N 50.0N	140 N 136 N 44 GN 46 GN	74,0N 70,0N 28,0N 26,0N
OUTPUT ACTIVE FROM CS1 OUTPUT ACTIVE FROM CS2 OUTPUT ACTIVE FROM MRD	(TDOAİ) (TDOAZ) (TAOAZ)	228.N 224.N 52.0N	200, N 198, N 48, ON	102.N 100.N 28.0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH1) (TDOH2) (TDOH3) (TPDH) (TRC) (TWC)	148.N 146.N 140.N 136.N 256.N	118 N 116 N 118 N 114 N 216 N	36,0N 36,0N 34,0N 32,0N 128.N
	TH	P16.N VIC1	192.N VTC2	120.N
A0 #24.8NA 2 1 #22,1NA 2 20,2NA 2.	2.5NA 1.0NA 2.4NA 2.5NA	2.77 V 2.80 V 2.84 V 2.83 V	=2,77 V =2,82 V =2,87 V =2,85 V	
A5 =22,7NA 2 A6 =22,5NA 2	2,0NA 1,2NA 2,3NA 1.8NA	2.85 V 2.78 V 2.79 V 2.81 V	22,83 V 22,83 V 22,83 V	

-			C 6 7 7	— — pri V
A1	NA1 و 22 ه	21.0NA	2,80 V	-2,82 v
A2	#21,9NA	22.4NA	2.84 V	#2,87 V
A3	-55-0NV	22.5NA	2.83 V	=2.85 V
A 4	=23,1NA	22.0NA	2.85 V	55,89 V
A5	∞22,7NA	21,2NA	2.78 V	. S6,S€
A6	-22,5NA	22,3NA	2.79 V	-2,83 V
A7	=55.6NV	21.8NA	2.81 V	-2.83 V
CS1	-22,1NA	21.7NA	2,85 V	-2,85 V
csa	#81.9NA	24.0NA	2.89 V	<u>+</u> 2,89 V
MWR	~82 _* 0NV	39,6NA	2,79 V	-2,81 V
MRD	-22.1NA	21.7NA	2.83 V	-2.81 V
DIU	=21,4NA	21,6NA	2.93 V	-2,89 V
DII	=21,6NA	21.4NA	2.91 V	-2.86 V
DIS	#22,5NA	22.1NA	2.93 V	#2,88 V
DI3	ANS.ES=	ANG.SS	2.91 V	#2.86 V

RCA	CDP182580	256 X 4	CMOS	STATIC	RAM	31	AUG	78	TEMP:
	4.2								PAGE
	מממ	DÖ1		ממ	ā		po	13	
VOL1 VOL2 VOH1 VOH2	115.MV 125.MV 4.82 V 9.75 V	120' 140' 4,82 9.75	, M V ! V	155 4,8	7,4 V		15	50, MV 50, MV 82 V 75 V	
IDN1 IDN2 IDP1 IDP2	6.40MA 15.3MA -2.23MA -4.93MA	6.05 13.8 -2.23 -4.95	A M A	5.1 12. 72.6 4.8			12	75MA 2.6MA 25MA 02MA	
1071 1072 1023 1024	206.NA 208.NA 202.NA 209.NA	208, 205, 204, 203,	NA NA	51. 51.	Pana Sana Pana Sana		50	71, NA 77, NA 73, NA 79, NA	
1025 1026 1027 1028	207 NA 206 NA 199 NA 210 NA	204, 216, 212, 206.	NA NA	209 217	NA NA NA NA		50 51	1, NA 14, NA 13, NA	
ILDP	5.80UA								
IL1 IL2 IL3	=40,0UA =20,0UA =40,0UA								

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PCA, C	DP18225D	256 X	4 CMOS	STATIO	RAM	31 /	NUG 78	TEMP:	125	C	
								PAGE	9 ()F	10
PASSED	GALPAT GALPAT GALPAT	(WIDE (TIGHT)		VCC=: VCC=:	VBJ						
PASSED	DATA RET	ENTION '	TEST								
				vcc =	4.5V		5 . 0 V		10	øv.	
DATA SI	S ACCESS ETUP TIME OLD TIME		(TAA) (TDS) (TDH))	235.N 24.0N 12.0N		205. 20.0 12.0	N	100 101 12.	ØN	
AUDRES:	S SETUP T S SETUP T S HOLD TI PULSE WID	ME IME	CTAS: (TAS: (TAH: (TWP:	27) •	6.00N 129.N 18.0N		6.00 198. -16.9 74.9	N N	4 . ? 60 . 6 . ? 4 4 .	ON Bon	
C52 SE	ETUP TIM ETUP TIM OLD TIME OLD TIME	E	(TCS) (TCS) (TCS) (TCS)	52) H1)	170.N 164.N 50.0N 54.0N		150, 144, 46,0 48,0	N N	80, 78, 30, 28.	ØN ØN	
րսպերդ	ACTIVE F	ROM CS2	(700/) (700/) (700/)	(2/	242.N 238.N 56.0N		214, 210, 50,0	N	114 112 30.	N.	
OUTPUT OUTPUT OUTPUT READ C'	HOLD FRO HOLD FRO HOLD FRO HOLD FRO YCLE TIME CYCLE TIM	M CS2 M MRD M MWR	100T) 100T) 100T) 100T) 10WT)	(2) (3) ()	152.N 148.N 140.N 138.N 256.N 224.N		120'. 118, 118, 116, 232,	M M M M	36, 36, 128	0 N	
	TIL	11	ГН	۷ ۱	.01		VICA				
A 0 A 1 A 2 A 3	-136.NA -132.NA -130.NA	1 ā 1 3	32.NA 26.NA 33.NA 30.NA	2. 2.	74 V 77 V 81 V 80 V		-2,75 V -2,79 V -2,85 V -2.83 V				
A4 A5 A6 A7	=132.NA =135.NA =135.NA =133.NA	12 13	27 NA 28,NA 50,NA 28,NA	2. 2.	83 V 76 V 77 V 79 V		-2,86 V -2,79 V -2,80 V -2,81 V				
CS1 CS2 MWR MRD	=135.NA =131.NA =131.NA =130.NA	13	27,NA 55,NA 52,NA 28,NA	5. . S	82 V 87 V 76 V 80 V		-2,83 V -2,88 V -2,79 V				
010 011 013	=128.NA =130.NA =131.NA	1 a 1 a	51 NA 98 NA 97 NA 99 NA	s. 5.	91 V 89 V 91 V 89 V		-2,88 V -2,84 V -2,86 V -2,83 V				
				_							

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RCA	CDP1822SD	256 X 4	CMOS STATIC RAM	31 AUG 78	TEMPI	125 C SN;	Ģ
					PAGE	10 OF 10	

	boø	DO1	200	003
VOLI	130.MV	135 MV	145.MY	145 MV
ADES	140,MV	155.MV	175 MV	170.MV
VOH1	4,80 V	4.80 V	4.80 V	4,80 V
AOHS	9.72 V	9.72 V	9.71 V	9,72 V
IDN1	5.75MA	5 45MA	5.10MA	5,15MA
TONE	13,6MA	12,4MA	11.0MA	11.3MA
IDP1	-2.00MA	42,03MA	#1,99MA	#5'05WY
IOP2	-4.42MA	-4.47MA	-4.32MA	-4-49MA
IOZ1	850.NA	874 N 1	853,NA	835, NA
10Z2	831.NA	865 NA	853,NA	826,NA 886,NA
1073	827 NA	863 NA	849,NA	827,NA
1024	826 NA	857.NA	853,NA	820.NA
1025	833.NA	872,NA	867,NA	844 NA
1026	847.NA	860,NA	867,NA	836, NA
1027	835.NA	870°, NA	854.NA	841,NA
IOZB	830.NA	861.NA	861.NA	824.NA
ILOP	30,0UA			
IL1	-115,UA			
ILZ	-120 UA			
IL3	-110.UA			
71 /L	75 . ΩUA			

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PASSED GALPAT (TIGH	T LIMITS) VO T LIMITS) VO	C=10V C=10V C=5V	REPRODUCIBII ORIGINAL PAG	
. MOOCH DAIN REIEMITO	·			
	VCC	× 4,5V	5 . Ø V	10,0V
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA) (TDS) (TDH)	200.N 24.0N 10.0N	170'N 18.0N 10.0N	75.0N 8.00H 12.0N
AUDRESS SETUP TIME AUDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WIDTH	(TAS1) (TAS2) (TAH) (TWP)	16,0N 98,0N -18,0N 70,0N	12.0N .86.0N =14.0N 60.0N	4.70N 42.0N -4.70N 36.0N
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS1) (TCSS2) (TCSH1) (TCSH2)	150 N 146 N 44 GN 46 QN	130 N 176 N 38 M 40 M 40 M	66,0N 62,0N 24,0N 22.0N
OUTPUT ACTIVE FROM COUTPUT ACTIVE FROM COUTPUT ACTIVE FROM M	S2 (TDOA2)	194.N 190.N 44.0N	168, N 166, N 40, ON	86,0N 82,0N 24,0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH1) (TDOH2) (TDOH3) (TPOH) (TRC) (TWC)	132.N 130.N 134.N 130.N 216.N 200.N	102,N 102,N 114,N 108,N 184,N	26,0N 26,0N 30,0N 112.N 112.N
IIL	IIH	VICI	Atcs	
A0 =1.90NA A1 =2.30NA A2 =1.60NA A3 =2.00NA	1,70NA 2,20NA 2,00NA 1,90NA	2.95 V 3.00 V 2.96 V 2.97 V	-2,94 V -3,00 V -3,00 V	
A4 -1.80NA A5 -1.80NA A6 -2.00NA A7 -1.50NA	2,00NA 1,50NA 1,80NA 2.10NA	2,99 V 2,95 V 2,97 V 2,97 V	-3,04 V -3,08 V -3,08 V	
CS1 =1.80NA CS2 =2.20NA MWR =1.80NA MRD =2.20NA	1,60NA 1,60NA 1,70NA 2.10NA	2.96 V 3.93 V 2.95 V	=2,98 V =3,03 V =2,96 V =2.98 V	
DIO -1.70NA DI1 -1.80NA DI2 -2.00NA DI3 -1.90NA	1,70NA 1,70NA 2,00NA 1,70NA	3.09 V 3.05 V 3.05 V 3.03 V	-3,01 V -2,99 V -3,01 V -3,02 V	

RCA	COPISSOSO	256 X 4 CMOS	STATIC RAM	31 AUG 78	ŤEMP i	25 C 8N1
					PĀGE	2 OF 10
	000	poi	son	003		
00H5 00H1 00F3 00F1	85.0MV 95.0MV 4.86 V 9.80 V	90.0MV 105.MV 4.86 V 9.80 V	95'.0MV 120,MV 4,86 V 9,79 V	95,8MV 120,MV 4,86 V 9,80 V		
ION1 ION2 IOP1 IOP2	8.65MA 19.7MA -2.78MA -6.07MA	8,15MA 17.9MA =2,79MA =6.11MA	7,55MA AMA 2,73MA MAIP. 5#	7.55MA 16.0MA 22.86MA -6.27MA		
1021 1022 1023 1024	18,7NA 21,3NA 19,2NA 16,9NA	21,9NA 18,8NA 19,9NA 23,3NA	16,000 18,90a 18,50a 15,50a	21,7NA 18,4NA 17,8NA 21,3NA		
1025 1026 1027 1028	24.0NA 24.0NA 23.7NA 23.1NA	16,5NA 17.2NA 16,7NA 17.0NA	21,2NA 21,1NA 20,5NA 20,6NA	17,2NA 16,9NA 16,9NA 16,9NA		
ILDP	⇔5.00UA					
IL1 IL2 IL3 IL4	#5,00UA #5,00UA #5,00UA #5,00UA					

RCA COP1822SD 256 X 4 CMOS STATIC RAM 31 AUG 78 TEMP: #20 C SN: 10

PASSED GALPAT (WIDE LIMITS) VCC=10V PASSED GALPAT (TIGHT LIMITS) VCC=10V PASSED GALPAT (TIGHT LIMITS) VCC=5V

	vcc	± 4.5V	S.øv	10.0V
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA) (TDS) (TDH)	200.N 24.0N 8.00N	165.N 20.0N 8.00N	70.0N 8.00N 10.0N
ADDRESS SETUP TIME ADDRESS SETUP TIME AUDRESS HOLD TIME WRITE PULSE WIDTH	(TAS1) (TAS2) (TAH) (TWP)	18,0N 96,0N +16,0N 72.0N	14.7N 80.7N ~12.7N 62.7N	4.70M 38.0N -2.00N 34.0N
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS1) (TCSS2) (TCSH1) (TCSH2)	148.N 146.N 42.ØN 44.ØN	176'N 122'N 36,0N 36.0N	52,0N 58,0N 62,0N 82,0N
OUTPUT ACTIVE FROM CS1 OUTPUT ACTIVE FROM CS2 OUTPUT ACTIVE FROM MRD	(TDOA1) (TDOA2) (TDOA3)	188.N 186.N 40.0N	160', h 158', h 36, mn	80,0N 78,0N 22.0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH1) (TCOH2) (TDOH3) (TPOH) (TRC) (TWC)	126.N 124.N 132.N 128.N 208.N 224.N	98.0N 96.0N 112.N 106.N 176.N 184.N	24,0N 24,0N 28,0N 28,0N 104,N 96,0N
IIL IT	Н	VICI	VICE	
A1 =400,PA 40 A2 =200,PA 30	0.PA 0.PA 0.PA 0.PA	3.00 V 3.04 V 3.01 V 3.02 V	-2,99 V -3,04 V -3,04 V	
A5 =300.PA 20 A6 =300.PA 30	0,PA 0,PA 0.PA 0.PA	3.04 V 3.00 V 3.01 V 3.01 V	-3,09 V -3,02 V -3,06 V -3,04 V	
CS2 \$400,PA 20 MNR =300.PA 20	0,PA 0,PA 0,PA 0,PA	3.01 V 3.04 V 2.98 V 3.01 V	-3,03 V -3,08 V -3,00 V -3,00 V	
DI1 =200.PA 30 DI2 =400.PA 40	0.PA 0.PA 0.PA 0.PA	3.13 V 3.10 V 3.10 V 3.08 V	-3,05 V -3,03 V -3,05 V -3,06 V	

RCA	CDP18228D	256 X 4 CMDS	STATIC RAM	31 AUG 78	TEMP	#20 C	SNI
					PÂGE	4 OF	10
	000	001	002	003		,	
VOL:	75,0MV	80,0MV	85. ØMV	85. gmv			
AOL5	₿Ø,ØMV	9ø.ømv	105,MV	105.MV			
VOHI	4.88 V	4,88 V	4.88 V	4,88 V			
VOH2	9.83 V	9 84 V	4,88 V 9.82 V	4,88 V 9,84 V			
IDNI	9.75MA	9'. RØMA	8 , 60MA	8, 55MA		٠	
ENGI	55.6MV	20.6MA	18,1MA	18.4MA			
IDP1	#3,27MA	+3,27MA	#3,26MA	-3,36MA			
IDP2	#7,10MA	=7.16MA	#6.98MA	≈7.36MA			
IOZi	6.90NA	1,10NA	6,40NA	#100 PA			
IOZZ	3,20NA	4 <u>,</u> 30 n a	3,00NA	2,60NA			
1023	4.70NA	3,50NA	S.SQNA	4,20NA			
IOZ4	8.10NA	600.PA	5.80NA	1 DONA			
1025	1.50NA	5,90NA	1.10NA	4, 90NA			
1026	1,60NA	6,10NA	1,20NA	4,50NA			
1027	1,70NA	5,70NA	1.20NA	4,60NA			
IOZ8	1.90NA	5.80NA	1,50NA	4.10NA			
ILDP	+10,0UA						
ILi	-5. 00UΛ						
IL2	#5.00UA						
IL3	5,00UA						
IL4	-5.00UA						

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PAGE 5 OF 10

PASSED GALPAT (WIDE LIMITS) VCC=10V PASSED GALPAT (TIGHT LIMITS) VCC=10V PASSED GALPAT (TIGHT LIMITS) VCC=5V

	vcc	# 4.5V	5 . 0 v	10°.00
ADDRESS ACCESS TIME	(TAA)	195.N	1601N	65.0N
DATA SETUP TIME DATA HOLD TIME	(TDS) (TDH)	30.0N 6.00N	22.0N 8.09N	8.70 10.0 10.0
ADDRESS SETUP TIME ADDRESS SETUP TIME	(TAS1) (TAS2)	16,0N	17.0N 74.0N	4.00N 34.0N
ADDRESS HOLD TIME	(TAH)	94,0N -16,0N	#12.ØN	-5*80N
WRITE PULSE WIDTH	(TWP)	76.0N	64. MN	32.0N
CS1 SETUP TIME	(TCSS1)	144.N	120 N	56,0N
CS2 SETUP TIME	(TCSS2)	142.N	118.N	54,0N
CS1 HOLD TIME	(TCSH1)	48, ØN	40 , 0N	ลอโดพ
CSP HOLD TIME	(TCSH2)	40'. ØN	40.0N	50,0H
OUTPUT ACTIVE FROM CS:		184.N	152,N	80,0N
OUTPUT ACTIVE FROM CS		185.N	148.N	78, ØN
OUTPUT ACTIVE FROM MRE) (TDOA3)	38.0N	34.0N	22.00
OUTPUT HOLD FROM CS1	(TDOH1)	120.N	90 _B 0N	55,00
OUTPUT HOLD FROM CS2	(TDOH2)	118.N	90. AN	22,ØN
OUTPUT HOLD FROM MWR	(TDOH3) (TPDH)	(32,N 126,N	110 N 106 N	58, 0N 88, 0N
READ CYCLE TIME	(TRC)	200 N	168,N	104.N
WRITE CYCLE TIME	(TWC)	232.N	176.N	96.0N
IIL :	IIH	VIC1	VICE	
	100.PA	3.06 V	-3,04 V	
	100.PA	3,10 V	+3,04 V +3,10 V +3,10 V	
	100,2A	3 76 V	#3,10 V #3,10 V	
-	100.PA	3.78 V	-3,10 V	
	LOØ.PA	3.10 V	-3,14 V	
	100,PA	3.05 V	=3,08 V	
	100°, PA 100°, PA	3.07 V 3.07 V	+3,12 V +3,11 V	
	•	,a _e c, v		
CS1 =100.PA 1	LOO PA	3.08 V	-3,09 V	
	0.00 A	3.11 V	-3,13 V -3,07 V	
	100,PA 100,PA	3,04 V 3,08 V	=3.07 V =3.08 V	
DIO 0.00 A 1	100.PA	3.18 V		
-	IND.PA	3.15 V	=3,11 V =3,10 V	
· · · · · · · · · · · · · · · · · · ·	0.00 A	3,15 V	-3,10 V -3,11 V	
	100,PA	3.14 V	-3.13 V	

RCA	CDP182RSD	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP:	⊕55 G	SNI
					PAGE	6 OF	10
	noø	001	poè	200			
VOHS VOHI VOLI	70.0MV 75.0MV 4.90 V 9.85 V	70,0MV 80,0MV 4,90 V 9,86 V	75 ØMV 90 ØMV 4 90 V 9 85 V	75,0MV 90,0MV 4,90 V 9,86 V			
ION1 IOP1 IOP2	10,8MA 25,4MA =3.80MA =8.26MA	10.3MA 23.3MA -3.85MA -8.38MA	9.65MA 20.7MA #3.84MA #8.15MA	9.60MA 20.9MA 43.95MA 8.58MA			·
10Z1 10Z2 10Z3 10Z4	3.80NA -100.PA 3.60NA 5.70NA	→100 PA 3 40NA 400 PA →1 90NA	3.90NA 300.PA 1.70NA 5.20NA	1,80NA 1,80NA 1,20NA 1,70NA			
1025 1026 1027 1028	-1,60NA -1,50NA -1,50NA -1,40NA	5,40NA 5,60NA 5,40NA 5,50NA	=1,70NA =1,80NA =1,80NA =1.80NA	4°70NA 4°50NA 4°90NA 4°70NA			
ILDP	-20.0UA						
TL1 TL2 TL3 TL4	#5,00UA #5,00UA #5,00UA						

									<u> </u>			
RCA	CDP182280	256 X	4	CMOS	STATIC	RAM	31	AUG 78	TEMP:	85 C	5N \$	10

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	LIMITS) VC	C=10V C=10V C=5V	REPRODUCIBI ORIGINAL PA	LITY OF THE GE IS POOR
PASSED DATA RETENTION	V TEST			
	VCC	≖ 4,5V	5 . 0V	10.0V
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA) (TDS) (TDH)	200.N 24.0N 12.0N	175.N 20.QN 12.QN	85 0N 8 00 14 0N
ADDRESS SETUP TIME ADDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WIDTH	(TAS1) (TAS2) (TAH) (TWP)	10.0N 106.N -18,0N 78.0N	8.00N 94.0N -14.0N 70.0N	4 . ØØN 48 . ØN - 4 . ØØN 40 . ØN
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS!) (TCSS2) (TCSH1) (TCSH2)	154.N 157.N 54.0N 54.0N	136 N 134 N 46 ON 48 ON	72,0H 70,0N 30,0N 28.0H
OUTPUT ACTIVE FROM CS OUTPUT ACTIVE FROM CS OUTPUT ACTIVE FROM MS	(SADOT) SE	202.N 200.N 48.0N	180, N 178. N 44, MN	96, ØN 94, ØN 28. ØN
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH1) (TDOH2) (TDOH3) (TPOH) (TRC) (TWC)	138.N 134.N 136.N 132.N 224.N 208.N	108/ N 196/ N 116/ N 110/ N 200/ N 184/ N	28,0N 30,0N 32,0N 120,N 120,N
IIL	IIH	VICI	VICP	
A0 =27,1NA A1 =29,2NA A2 =27,4NA A3 =28.6NA	27.5NA 28.6NA 28.1NA 27.8NA	2.94 V 2.98 V 2.95 V 2.96 V	#2,93 V #2,99 V #2,99 V	
A4 =27,0NA A5 =28,0NA A6 =29,1NA A7 =27,2NA	27,8NA 26,4NA 28,4NA 29,4NA	2.98 V 2.94 V 2.96 V 2.96 V	93,03 V 92,97 V 93,00 V 92,99 V	
CS1 = 28,3NA CS2 = 28,2NA MWR = 26,5NA MRD = 28.1NA	26.3NA 26.8NA 26.1NA 27.5NA	2.95 V 2.98 V 2.91 V 2.94 V	#2,97 V #3,02 V #2,94 V	
DIØ =27,1NA DI1 =26.9NA DI2 =27,0NA DI3 =27.4NA	28.1NA 27,4NA 27,6NA 27,1NA	3.08 V 3.04 V 3.04 V 3.02 V	#2,99 V #2,98 V #2,99 V #3.01 V	

RCA	CDP1822SD	256 X 4 CMDS	STATIC RAM	31 AUG 78	TEMP	85 C SNT
					PAGE	8 OF 10
	Daø	DO1.	noz	003		
VOL1 VOH1 VOH2	100.MV 115.MV 4.83 V 9.76 V	105.MV 125.MV 4.84 V 9.76 V	115.MV 145.MV 4.82 V 9.75 V	115 MV 140 MV 4 84 V 9.76 V		
IDN1 IDN2 IDP1 IDP2	7.30MA 16.6MA -2.32MA -5.10MA	6.90MA 15.1MA -2.33MA -5.12MA	6.40MA 13.2MA #2.29MA #4.99MA	6.40MA 13.5MA -2.39MA -5.27MA		
1021 1022 1023 1024	203,NA 195,NA 199,NA 193,NA	195, NA 200, NA 196, NA 200. NA	185.NA 182.NA 182.NA 185.NA	185,NA 180,NA 183,NA 178.NA		
1025 1026 1027 1028	199.NA 199.NA 207.NA 195.NA	201.NA 196.NA 191.NA 202.NA	188,NA 195,NA 191,NA 187,NA	189,NA 174,NA 185,NA 181,NA		
ILDP	⇔5,00UA					
IL1 IL2 IL3 IL4	AU0,05# AU0,05# AU0,05# AU0,05#					

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PASSED	GALPAT	(WIDE	LIMITS)	ACC*10A
PASSED	GALPAT	(TIGHT	LIMITS)	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS)	VCC*5V

	, ,			
	vcc	= 4.5V	5 * Ø V	10.8V
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA) (BCT) (TDH)	215.N 24.0N 12.0N	190', N 20.0N 12.0N	95 0N 8 0N 14 0N
ADDRESS SETUP TIME ADDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WIOTH	(TAS1) (TAS2) (TAH) (TWP)	8.00N 114.N -18.0N 82.0N	8.00M 104.N -15.0N 72.0N	4.00N 56.0N -6.00N 44.0N
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS1) (TCSS2) (TCSH1) (TCSH2)	164.N 158.N 54.0N 56.0N	144, N 142, N 48, N 50. N	80,00 78,00 30,00 30.00
OUTPUT ACTIVE FROM CS OUTPUT ACTIVE FROM MR	(SACOT) S	218.N 214.N 52.0N	194°N 192°N 48°N	106.N 104.N 30.0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH1) (TDOH2) (TDOH3) (TPOH) (TRC) (TWC)	140 N 138 N 138 N 134 N 232 N 224 N	110°N 108°N 118°N 118°N 208°N	32,0N 34,0N 36,0N 36,0N 128,N
IIL	IIH	VIC1	VICS	
AU =164 NA A1 =169 NA A2 =165 NA A3 =164 NA	159, NA 160, NA 160, NA 158, NA	2,95 V 2,99 V 2,96 V 2,97 V	94 V 93,00 V 93,00 V	
A4 = 158, NA A5 = 167, NA A6 = 170, NA A7 = 165, NA	154, NA 157, NA 163, NA 164, NA	3'00 V 2.95 V 2.97 V 2.97 V	73,04 V 72,98 V 73,00 V	·
CS1 = 166.NA CS2 = 162.NA MWR = 157.NA MRD = 161.NA	151, NA 156, NA 149, NA 153, NA	2.95 V 2.99 V 2.91 V 2.95 V	72,98 V 73,95 V 72,97 V	
DIØ #160.NA DII #160.NA DI2 #158.NA DI3 #157.NA	161,NA 159,NA 154.NA 156.NA	3.10 V 3.06 V 3.05 V 3.03 V	3,01 V =2,99 V =3,00 V =3,02 V	

RCA	CDP18225D	256 X 4	CMOS	STATIC RAM	31	AUG 78	TEMP:	125 C	SNI	10
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	กอุด	001	poż	003
AOFS AOF?	115.MV 130.MV	120 MV 145 MV	130.MV 165.MV	130, MV 160, MV
AOHI	4.80 V	4,81 V	4.81 V	4,82 V
ADH5	9.72 V	9.72 V	9.72 V	9.73 V
IDN1	6 . 50MA	6.15MA	5.70MA	5,70MA
IDNS	14.8MA	13.3MA	11,7MA	11.9MA
IDP1	#2.Ø7MA	-2,11MA	#2,07MA	-2,13MA
IDPZ	#4.56MA	-4.61MA	=4.45MA	-4.72MA
1071	849.NA	813, NA	790.NA	732', NA
Ioza	834.NA	816,NA	787 NA	725,NA
IUZ3	835.NA	806 NA	784 NA	728, NA
1074	828.NA	812.NA	787.NA	722.NA
1025	842 NA	824' _e NA	805.NA	745 NA
1026	838.NA	814, NA	806, NA	724,NA
IOZ7	847 NA	809, NA	799 NA	733, NA
1028	833.NA	817.NA	793.NA	725.NA
ILDP	40.0UA			
IL1	#95.0UA			
IL2	#115.UA			
IL3	#90.0UA			
IL4	=75 .ØU∧			

PAGE 1 DF 10

PASSED GALPAT	(WINE LIMITS)	VCC=10V	
PASSED GALPAT	(TIGHT LIMITS)	VCC=10V	REPRODUCIBILITY OF THE
PASSED GALPAT	(TIGHT LIMITS)	VCC=5V	ORIGINAL PAGE IS FOOR

THOSED DATA METERITUM	1291			
	vcc	= 4.5V	5.0v	10.0v
ADDRESS ACCESS TIME	(TAA)	230.N	190'.N	75.0N
DATA SETUP TIME	(708)			
		18,0N	16.ØN	8.00N
DATA HOLD TIME	(404)	12.0N	12.0N	12.0N
ADDRESS SETUP TIME	(TAS1)	8.00N	8.0MN	4.001
ADDRESS SETUP TIME	(TAS2)	112.N	92,0N	40 ØN
ADDRESS HOLD TIME	(TAH)	-16 GN	#12.0N	-2.00M
WRITE PULSE WIDTH	(TWP)	95°0N	52.0N	32 0N
Busic Gede Manill	L i Ri J	0 6 9 814		35,610
CS1 SETUP TIME	(TCSS1)	136.N	118, N 116, N	58, ØN
CS2 SETUP TIME	(TCSS2)		116.N	56,0N
CS: HOLD TIME	(TCSH1)	132.N 38.0N	34.7N	22,0N
CS2 HOLD TIME	(TCSH2)	40 ON	34.0N	25.0N
, , , , , , , , , , , , , , , , , , ,	• • • • • • • • • • • • • • • • • • • •		_	u = # 5 · ·
OUTPUT ACTIVE FROM CS		356°N	188, N	84,0N
OUTPUT ACTIVE FROM CS.		224.N	186.N	82, ØN
OUTPUT ACTIVE FROM MR	D (TDDA3)	46. ØN	40 an	22.ØN
OUTPUT HOLD FROM CS1	(IHOQT)	140 m	110 N	30,00
OUTPUT HOLD FROM CS2	(TDOH2)	138.N	108, N	30,0N
OUTPUT HOLD FROM MRD	(TDOH3)	138 N	116 N	28, ØN
OUTPUT HOLD FROM MWR	(TPDH)	134.N	110,N	28,00
READ CYCLE TIME	(TRC)	240 N	200, N	104 N
WRITE CYCLE TIME	(TWC)	176 N	160 N	96. ØN
IIL :	IIH	VIC1	VTC2	
A0 .2.90NA	2,80NA	3,20 V	=3,19 V =3,26 V =3,27 V	
	3.10NA	3,25 V	-3 3A V	
the state of the s	2,60NA	3.85 V	-3 27 V	
	2.60NA	3.25 V	-3.28 v	
m g · D · Q ·		• • • • •		
A4 #2.70NA 2	2,70NA	3.27 V	#3,29 V +3,29 V	
	2,80NA £	3.17 V	-3'22 V	
	2,40NA	3.17 V	-3,21 V	
A7 =2.60NA	2.50NA	3.17 V	#3.20 V	
664 a cana	7.7004	79 mben 11	i a t a a a a	
	2.70NA	3.20 V	-3,18 V -3,24 V -3,16 V	
CS2 #2,60NA 2	2,70NA	3,22 V	-3,24 V	
MWR ⇔2.70NA 8 MRD ⇒3.00NA 8	2,60NA	3,17 V	-3,16 V	
MRD =3.00NA	2.70NA	3.21 V	⇒3,20 V	
DIØ =2,50NA 3	3.10NA	3128 V	-3,23 V	
	2,50NA	3,26 V		
	E,50NA	3,25 V	=3,21 V =3,21 V	
· •	2.30NA	3.25 V	-3.20 V	
	- P - A KILL H	neca A	93.E0 A	

RCA	CDP1822SD	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP!	25 C SN: 11
					PAGE	2 OF 10
	DOØ	DOI	002	D03		•
AOH5 AOH1 AOF5 AOF1	90.0MV 95.0MV 4.87 V 9.81 V	95.0MV 105.MV 4.87 V 9.81 V	100 MV 115 MV 4 86 V 9 80 V	100, MV 115, MV 4, 87 V 9, 81 V		
IDN1 ION2 IOP1 IDP2	7.90MA 19.8MA =2.94MA =6.47MA	7,50MA 18,6MA -2,96MA -6,51MA	7.10MA 16.1MA +2.89MA +6.23MA	7.10MA 16.4MA #2,99MA #6.61MA		
IOZ1 IOZ2 IOZ3 IOZ4	17,7NA 14,0NA 15,8NA 19,0NA	11,6NA 14,2NA 13,2NA 10,5NA	17, 9NA 14, 4NA 14, 6NA 18, 3NA	10.6NA 13.5NA 14.0NA 10.8NA		
1025 1026 1027 1028	12,1NA 12,4NA 12,1NA 12,0NA	16,9NA 16,6NA 16,6NA 16,1NA	12,4NA 12,4NA 12,3NA 12,6NA	15,3NA 15,5NA 15,1NA 15,0NA		
ILDP	#15,0UA					
IL1 IL2 IL3 IL4	⇔5,00UA ⇔10,0UA ⇔10,0UA ⇔5,00UA					

PASSED	GALPAT	(WIDE	LIMITS)	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS)	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS)	VCC=5V

PASSED DATA RETENTION TEST

	vcc	# 4.5V	5'.ØV	10',0V
ADDRESS ACCESS TIME	(TAA)	250.N	185, N	65.0N
DATA SETUP TIME	(TOS)	20.0N	16, GN	6.00N
DATA HOLD TIME	(TDH)	10.0N	10, ON	10.0N
ADDRESS SETUP TIME	(TAS1)	12'.0N	10,0N	4.00N
ADDRESS SETUP TIME	(TAS2)	114.N	92.0N	34.0N
ADDRESS HOLD TIME	(TAH)	-16.0N	=12.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	64.0N	56.0N	30.0N
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS1)	134 N	116,N	54,0N
	(TCSS2)	130 N	112,N	54,0N
	(TCSH1)	32 ON	30,0N	20,0N
	(TCSH2)	34 ON	30,0N	18,0N
OUTPUT ACTIVE FROM CS	(SAOGT) S	240 N	190'N	80,0N
OUTPUT ACTIVE FROM CS		238 N	188'N	78,0N
OUTPUT ACTIVE FROM MR		42.0N	38.0N	22.0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH1)	134.N	102, N	30,0N
	(TDOH2)	132.N	102, N	30,0N
	(TDOH3)	136.N	114, N	26,0N
	(TPOH)	132.N	108, N	28,0N
	(TRC)	224.N	192, N	104.N
	(TWC)	176.N	160, N	96.0N
IIL	11H	VICI	AICS	
	300.PA 500.PA 300.PA 300.PA	3.25 V 3.30 V 3.30 V 3.30 V	#3,24 V #3,30 V #3,32 V #3,32 V	
A4 +300.PA	300,PA	3.32 V	#3,34 V	
A5 +300.PA	300,PA	3.23 V	#3,27 V	
A6 +500.PA	300,PA	3.22 V	#3,26 V	
A7 +300.PA	300.FA	3.22 V	#3,25 V	
ES2 #300.PA MWR =300.PA	400 PA 300 PA 200 PA 400 PA	3.25 V 3.28 V 3.22 V 3.26 V	-3,23 V -3,28 V -3,21 V -3,25 V	
	400°, PA 300°, PA 300°, PA 300°, PA	3.33 V 3.31 V 3.30 V 3.30 V	#3,27 V #3,25 V #3,26 V #3,25 V	

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RÇA	CDP1822SD	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP:	-20 C	SNI	ıī
					PAGE	4 OF 1	Ø	
	000	DOI	poe	003				
VOL1 VOL2 VOH1	80.0MV 80.0MV 4.88 V	85.0MV 90.0MV 4.89 V	90'.0MV 100.MV 4.89 V	90.0MV 100.MV 4.89 V				
VOHE	9,84 V	9' 84 V	9.84 V	9.84 V				
IDN1 IDN2 IDP1	8,80MA 22,6MA #3,44MA	8.35MA AM3.05 AM02.25	8.90MA 18.6MA #3.41MA	7.95MA 18.8MA 51MA				
IDPS	-7.57MA	-7.66KA	₩7.38MA	-7.75MA				
IOZ1 IOZ2 IOZ3	7.60NA 7.60NA 800.PA	1.80NA -400.PA 7.20NA	5,60NA 7,70NA 600,PA	2.49NA 200.PA 7,50NA				
1024	3,10NA	4.60NA	2.40NA	5.60NA				
1025 1026	5.60NA 5.80NA	1.70NA 1.30NA	6,40NA 6,40NA	600, PA 700, PA				
1027 1028	5.70NA 5.90NA	1,50NA 1.00NA	6,40NA 6.50NA	500,PA 600,PA				

ILDP	-5 ,00U∧
IL1 IL2 IL3 IL4	#5.00UA #5.00UA #5.00UA
	•

RCA	COP1822SO	256 X 4	CHOS STATIC	RAM 31	AUG 78	TEMPS	#55 C	SNI	11
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(WIDE LIMITS) VCC=10V (TIGHT LIMITS) VCC=10V

PASSED GALPAT PASSED GALPAT PAGE 5 OF 10

PASSED GALPAT (TIGHT PASSED GALPAT (TIGHT	'LIMITS) VC	C=10V C=5V	REPRODUCIBILIT ORIGINAL PAGE	
PASSED DATA RETENTION	I TEST			TO A WHAT
	VCC	* 4.5V	5 . øv	10'-0V
ADDRESS ACCESS TIME	(TAA)	245.N	180'.N	65.0N
DATA SETUP TIME	(TDS)	24.0N	18.0N	6.00N
DATA HOLD TIME	(TDH)	8.00N	8.00N	10.0N
ADDRESS SETUP TIME ADDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WIDTH	(TAS1)	12.0N	8'.00N	4.00N
	(TAS2)	114.N	.88.0N	32.0N
	(TAH)	-16.0N	.12.0N	=2.00N
	(TWP)	-66.0N	.56.0N	28.0N
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS1) (TCSS2) (TCSH1) (TCSH2)	134.N 130.N 38.ON 38.ON	110,N 110,N 32,0N 32,0N	18.0N 50,0N 52,0N
OUTPUT ACTIVE FROM CS	(SACOT) Si	240, N	182, N	76,0N
OUTPUT ACTIVE FROM CS		238. N	180, N	74,0N
OUTPUT ACTIVE FROM MR		40.0N	34, ON	20,0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TOOH!) (TOOH2) (TOOH3) (TPOH) (TRC) (TWC)	130.N 128.N 134.N 132.N 208.N 184.N	98,0N 96.0N 112,N 108,N 176,N 160.N	28,00 26,00 26,00 96,00 98.00
IIL	ITH	VIC1	Vīcā	
A0 #100.PA	100.PA	3.30 V	53,29 V	
A1 #100.PA	100.PA	3.36 V	53,36 V	
A2 #100.PA	100.PA	3.36 V	53,37 V	
A3 0.00 A	100.PA	3.36 V	53,37 V	
A4 -100.PA	100,PA	3,37 V	-3,38 V	
A5 -100.PA	100,PA	3.28 V	-3,32 V	
A6 -100.PA	100,PA	3.27 V	-3,31 V	
A7 -100.PA	100,PA	3.28 V	-3,30 V	
CS1 = 100.PA	100.PA	3.30 V	#3,29 V	
CS2 = 100.PA	100.PA	3.33 V	#3,34 V	
MWR = 100.PA	0.00 A	3.27 V	#3,27 V	
MRD = 100.PA	100.PA	3.31 V	#3,30 V	
DIØ 0.00 A	100,PA	3.38 V	+3,32 V	
DII *100.PA	100,PA	3.36 V	+3,30 V	
DI2 =100.PA	100,PA	3.36 V	+3,31 V	
DI3 0.00 A	100,PA	3.36 V	+3,29 V	
		B-105		

RCA	COP182250	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP	#55 C	SN:	11
					PAGE	6 OF	10	
	noø	DO1	soa	203				
045 047 067 067	80.0MV 75.0MV 4.90 V 9.86 V	85.0MV 80.0MV 4.90 V 9.86 V	85,0MY 90,0MV 4,90 V 9,85 V	85,0MV 90.20 4,90 V 9.86 V				
ION1 ION2 IOP1 IOP2	9,55MA 24,8MA 44,00MA 8,73MA	9'.15MA 23.0MA #4.00MA #8.82MA	8.75MA 20.8MA -3.96MA -8.53MA	8,70MA 21,1MA 4,09MA 8,97MA				
1071 1072 1073 1074	4.60NA 600.PA 3.10NA 5.90NA	-700'.PA 2'.70NA 1,00NA -1.70NA	4,80NA 1,30NA 1,50NA 5,40NA	=1,60NA 1,10NA 1,80NA =1.30NA				
1025 1026 1027 1028	#1.30NA #1.20NA #1.30NA #1.30NA	5,10NA 5,50NA 5,30NA 5.50NA	=1.10NA =1.20NA =1.30NA =1.30NA	4,40NA 4,40NA 4,80NA 4,70NA				
ILDP	#15.0UA							
IL1 IL2 IL3 IL4	-5.00UA -5.00UA -5.00UA -5.00UA							

RCA	CDP1822SD	256 X 4	CHOS	STATIC	RAM	31 AUG	78	TEMP:	85 C	SNI	1 i
								PAGE	7 DF	10	
	5 55	4									

PASSED	GALPAT	(WIDE	LIMIYS)	VCC=10V
PASSED	GALPAT	CTIGHT	LIMITS)	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS)	VCC=5V

PASSED DATA RETENTION	TEST			
	vcc	≈ 4,5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	215.N	185 N	ลดู ็ตุง
DATA SETUP TIME	(TDS)	199.N	16.0N	8 . ØØN
DATA HOLD TIME	(TDH)	18.0N	16.0N	14.0N
Manager and Company of the Paris of the Pari	V	1.0 2 0 1	108444	, , , , ,
ADDRESS SETUP TIME	(TAS1)	6.00N	6.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	108 N	92.0N	44.01
ADDRESS HOLD TIME	(TAH)	-14,0N	-12 ON	-2,00N
WRITE PULSE WIDTH	(TWP)	66.0N	60.0N	36.0N
THE PLANT OF GREAT WARRY		30404	C2 50 M 17 3 4	a g 2014
CS1 SETUP TIME	(TCSS1)	140.N	122,N	64 ON
CS2 SETUP TIME	(TCSS2)	138 N	120.N	62, ØN
CS1 HOLD TIME	(TCSH1)	42. NN	38.0N	24,00
CS2 HOLD TIME	(TCSH2)	46 ØN	40.0N	24.0N
OPE HOLD JAIN	(LCOHE)	40.2014	of at \$ At IA	हिला ∎ धाप
OUTPUT ACTIVE FROM CS1	(TDOA1)	218.N	188 N	90,0N
OUTPUT ACTIVE FROM CS2	(TDOAZ)	216.N	186.N	
OUTPUT ACTIVE FROM MRD	(TDOAZ)	46.0N	42.ØN	90,0N 86.0N
OUT OF ACTIVE TRUM MAD	CEMBULL	14 C = 614	et CE ≅ K₁ (A	SB • Min
DUTPUT HOLD FROM CS:	(TDOH1)	142 N	112,N	32,0N
OUTPUT HOLD FROM CS2	(SHOOT)	138 N	1 1 12 5 14	
OUTPUT HOLD FROM MRD	(TDOHE)	138,N	108 N	32,0N
OUTPUT HOLD FROM MWR	(TPDH)		110 a N	30,0N
READ CYCLE TIME		134.N	116,N 110,N 208,N 176.N	30.0N
WRITE CYCLE TIME	(TRC)	240 N	ድማር _ት ህ	112.N
METIC CIPTO 1700	(TWC)	192.N	INDAN	112.N
IIL II	IH	VICI	VICE	
A. De This is	4 794.1.0	m	·	
		3,19 V	-3,18 V	
		3.24 V	-3,25 V	
		3.24 V	95°5% ∧	
A3 =38.7NA 39	9.5NA	3.82 A	-3.27 V	
A4 =39,4NA 39	9 . Ø N A	7 34 V		
		3.26 V	-3,28 V	
. <i>f</i> =	7,6NA	3.16 V	=3,21 V	
	9.2NA	3.16 V	#3,50 A	
A7 =40.7NA 40	%_2NA	3.16 V	-3.18 V	
CS1 *38,7NA 38	B,3NA	3.18 V	-3,17 V	
			## # T V	
F		3,21 V	*3,23 V	
		3,15 V 3,19 V	÷3,15 V ⇒3,19 V	
tite maskalaw 20	M 9 F E. O C.	Ja17 Y	⇒oela A	
010 =38,7NA 41	i "6NA	3.27 V	.3,22 V	
DI1 -39,0NA 39	•		#3,19 V	
		3.24 V 3.24 V		
			-3,20 V	
073 -21 *10W 20	OBTIAN	3.24 V	⇒3°19 V	
		_		

RCA	CDP18225D	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP	85 C S
					PĀGE	8 OF 10
	000	001	noż	003		
VÖL1 VOL2 VOH1 VOH2	105.MV 110.MV 4.84 V 9.77 V	110 MV 125 MV 4 84 V 9 77 V	120,MV 140,MV 4,84 V 9,76 V	180, MV 135, MV 4,84 V 9,78 V		
ION1 ION1 IOP1 IOP2	6.85MA 16.9MA =2.48MA =5.45MA	6.50MA 15.3MA -2,50MA -5.49MA	5.15MA 13.7MA -2.44MA -5.31MA	6,15MA 13,9MA 72,54MA 75,58MA		
1021 1022 1023 1024	#34,1NA #37,1NA #49,6NA #45,4NA	=46,8NA =54,0NA =50,6NA =52,6NA	#45,7NA #44,1NA #55,7NA #53,9NA	#48,2NA #53,6NA #50,1NA #51,0NA		
1025 1026 1027 1028	#43,9NA #45,6NA #47,4NA #46,0NA	+56,5NA +57,4NA +58,5NA +55,6NA	#50,8NA #52,0NA #52,8NA #51.8NA	-56,7NA -56,7NA -56,5NA -57,0NA		
ILDP	-10.0UA					
IL1 IL2 IL3 IL4	#40,0UA #55,0UA #35,0UA #30,0UA					

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PASSED GAL	PAT (WIDE	LIMITS)	VCC=1ØV	THE THE
PASSED GAL	.PAT (TIGHT .PAT (TIGHT	LIMITS	VCC=10V VCC=5V	REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR
· consum some	er ne - Çeşwire	Ar Mirital Co.	,00-2.	OKIGENAL

PASSED DATA RETENTION TEST

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I MOOCO PAIR ACIENITUM	1501			
	VCC	= 4,5V	5'. ØV	10°.00
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA) (TDS) (TDH)	28,0N 28,0N 28,N	195'N 16'0N 18'0N	90 - 0 N 8 - 0 0 N 16 - 0 N
ADDRESS SETUP TIME ADDRESS SETUP TIME ADDRESS HOLD TIME	(TAS1) (TAS2) (TAH)	4.00N 122.N -12.0N	4.00N 104.N -12.0N	4.00N 52.0N -2.00N
WRITE PULSE WINTH	(TWP)	68. ØN	62.ØN	38,0N
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TC\$S1) (TC\$S2) (TC\$H1) (TC\$H2)	148 N 144 N 42 ON 46 ON	130, N 126, N 38, ON 40, ON	70,0H 68,0H 24,0H 24.0H
OUTPUT ACTIVE FROM CS1 OUTPUT ACTIVE FROM MRD	(SAOUT)	232.N 230.N 50.0N	202 N 200 N 44 ON	98,0N 98,0N 98,0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOHÍ) (TDOH2) (TDOH3) (TPDH) (TRC) (TWC)	142.N 140.N 138.N 136.N 248.N 208.N	114, N 110, N 116, N 112, N 216, N 184, N	34,0N 34,0N 32,0N 32,0N 120.N
III. I	TH.	VIC1	VTCR	
A1 =236,NA 2 A2 =232,NA 2	33.NA 31.NA 29,NA 25.NA	3.20 V 3.26 V 3.25 V 3.25 V	-3,29 V -3,28 V -3,29 V	
A5 =232,NA 2 A6 =237,NA 2	21,NA 231,NA 27,NA 32,NA	3.27 V 3.17 V 3.17 V 3.17 V	-3,29 V -3,22 V -3,21 V -3,19 V	
CS2 #224.NA 2 MWR #222.NA 2	19,NA 28,NA 17,NA 20,NA	3.19 V 3.22 V 3.15 V 3.20 V	-3,17 V -3,23 V -3,16 V -3,19 V	
210°4284 510 310 410	33.NA 26.NA 25.NA 20.NA	3.28 V 3.25 V 3.24 V 3.24 V	#3,23 V #3,20 V #3,19 V	

RCA	CDP18228D	256 X 4 CMOS	STATEC RAM	31 AUG 78	TEMP:	125 C	SNI
					PAGE	10 OF	10
	DOB	001	202	003			
00H2	115.MV 125.MV 4.82 V 9.74 V	125, MV 140, MV 4,82 V 9,74 V	135.MV 160.MV 4.82 V 9.73 V	135 MV 155 MV 4 82 V 9.74 V	·		
IDN1 IDN2 IDP1 IDP2	AMOS.8 AM15.21 AM45.22 AM488.4	5,85MA 13,6MA -2,26MA -4,95MA	5.55MA 12.2MA =2.21MA =4.75MA	5,55MA 12,4MA +2,29MA =4,99MA			
1021 1022 1023 1024	#751.NA #758.NA #771.NA #764.NA	+761 NA +775 NA +779 NA -784 NA	=752,NA =751,NA =762,NA =760,NA	#738, NA #744, NA #750, NA #749, NA			
1025 1026 1027 1028	-762,NA -770,NA -779,NA -774,NA	=775,NA =797,NA =782,NA =788,NA	₩762.NA ₩775.NA ₩778.NA ₩768.NA	+760, NA +748, NA +746, NA +757, NA			
ILDP	80.0UA						
IL: IL: IL: IL: IL:	-200.UA -260.UA -155.UA -130.UA						

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RCA	CDP182250	256 X 4	CMOS	STATIC	RAM	31	AUG 78	TEMP!	25 C	SN:	12
								PAGE	i OF	10	

PASSED	GALPAT	(WIDE	LIMITS)	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITSI	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS)	VCC=5V

PASSED DATA RETENTION	TEST			
	vcc	= 4.5V	5.0V	10'.0V
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA) (BDT) (HDT)	215.N 22.0N 12.0N	185′.N 18,0N 10,0N	75,0N 8,00N 12,0N
ADDRESS SETUP TIME ADDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WIDTH	(TAS1) (TAS2) (TAH) (TWP)	14.0N 106.N -14.0N 64.0N	10.0N 90.0N 912.0N 56.0N	4.00 42.00 42.00 44.00
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS1) (TCSS2) (TCSH1) (TCSH2)	150 N 180 N 180 N 38 0N	130'N 154'N 32.0N 0.00	62.0N 74.0N 22.0N 6.00
OUTPUT ACTIVE FROM CS OUTPUT ACTIVE FROM MR	(1AOOT) 1 (SAOOT) 5	208 N 238 N 46.0N	176'N 200'N 40.0N	84,0N 94,0N 24,0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH1) (TDOH2) (TDOH3) (TPOH) (TRC) (TWC)	136 N 194 N 136 N 132 N 224 N 248 N	108 N 164 N 114 N 110 N 200 N 176 N	30,000 58,000 30,000 112,00
	IIH	VICI	Aics	
A1 w1,90NA A2 #2,30NA	1,50NA 2,00NA 2,20NA 1,40NA	2,91 V 2,91 V 2,94 V 2,95 V	#2,89 V #2,95 V #2,95 V	
A5 #1,90NA	2,00NA 1,60NA 1,60NA 1.70NA	2.97 V 2.86 V 2.86 V 2.86 V	#2,96 V #2,91 V #2,91 V	
C82 =2.50NA MWR =2.90NA	1,80NA 1,40NA 1,50NA 1,60NA	2.91 V 4.96 V 2.89 V 2.89 V	-2,91 V -4,95 V -2,89 V -2,88 V	
DI1 +2,30NA DI2 +1,70NA	1,60NA 1,90NA 1,60NA 1.60NA	2.97 V 2.94 V 2.96 V 2.94 V	#2,91 V #2,92 V #2,89 V	

RCA	CDP18225D	256 X 4 CMQS	STATIC RAM	31 AUG 78	TEMP	25 C	\$N
				·	PAGE	2 OF	10
	000	001	ŠOO	003		·	
VOL1 VOH1 VOH2	90,0MV 95.0MV 4,86 V 9,80 V	95,0MV 110,MV 4,86 V 9,80 V	105.MV 130.MV 4.86 V 9.79 V	195, MV 120, MV 4,86 V 9,80 V	·		
IDN1 IDN2 IDP1 IDP2	#2#83WV	7.55MA 17.4MA -2.83MA -6.22MA	6.85MA 14.9MA =2.79MA =6.02MA	7.10MA 15.7MA -2.86MA -6.34MA			
1071 1072 1073 1074	20,0NA	21,2NA 22.9NA 25.8NA 27.8NA	24,7NA 22,3NA 18,0NA 21,1NA	19,2NA 19,8NA 24,9NA 21.5NA			
1025 1026 1027 1028	19,9NA 20,1NA	24,8NA 25,5NA 25.0NA 25,3NA	20,0NA 20,0NA 20,0NA 20,0NA	23,1NA 22,5NA 22,3NA 22,4NA			
ILDP	1.00UA						
IL1 IL2 IL3 IL4	-5.00UA -10.0UA -5.00UA -5.00UA						

71	AGE	3	OF	10

		•						PAGE	3	OF	10
PASSED PASSED PASSED	GALPAT	(WIDE (TIGHT (TIGHT		A C t	=10V =10V		REPRODU ORIGINAL	oibility Page is	of Po	THE OR	ŗ
PASSED	DATA R	ETENTION	TEST								
				vcc	s å,	έγ	5 . ØV		10	, øv	ŧ
DATA SE	S ACCESS ETUP TIN OLD TIME	ME	CTAA CTDS CTDH	3	24	7 N 6 N 6 N	180°,1 80°,1 10°,01	1	8 .	90N	ļ
			(TAS (TAS (TAH) (TNP)	2))	10; 014,	9N 1 N 9N 9N	12,01 18,08 10,01 10,82	1	38	00N	j j
CS2 SE			(TCS: (TCS: (TCS:	SŽ) Hį)	189	8 . N 8 . N . ØN 8 Ø	124'r 152'r 37'01 0'01	1	7 @ 2 2	, ØN	1
OUTPUT OUTPUT	ACTIVE	FROM CS	e troo.	(5A	219 239 42	ž.N	170,1 192,1 36,01	4	86 22	2 0 N	} Į
OUTPUT OUTPUT OUTPUT READ CY WRITE (HOLD FR HOLD FR	ROM CSE ROM MRD ROM MWR ME	(TDO!) (TDO!) (TDO!) (TRO!)	H2) H3) H)	134 176 134 126 246	I n N B n N B n N	1904 1467 1127 1984 1844 1844	₹ 	## 28 28	0 0 N N N N N N N N N N N N N N N N N N	! ; ;
	IIL		IIH		VIC1		vicā				
AØ A1 A2 A3	-400.P/ -300.P/ -400.P/	A '	300,PA 500,PA 500,PA 300.PA		3,00 3,00 3,03 3,04	V	72,78 V 75,01 V 75,04 V				
A4 A5 A6 A7	-300.P/ -400.P/ -300.P/	A	400, PA 300, PA 300, PA 300, PA		2,95	A A A	73,04 V 73,00 V 73,00 V 73,07 V				
CS1 CS2 MWR MRD	=200.P/ =700.P/ =600.P/	A :	400', PA 300, PA 300, PA 400. PA		3,00 4,96 2,98 2,99	A A A	73,00 V 74,95 V 72,99 V 72,97 V				
DIØ DI1 DI2 DI3	-400.P/ -500.P/ -400.P/)	300,PA 400,PA 300,PA 400.PA		5.06 3.04 3.05 3.03	V V V	3,00 V +3,00 V +3,01 V +3,01 V				
					T * * *	~					

RCA	CDP1822SD	256 X 4 CMOS	STATEC RAM	31 AUG 78	TEMP	⇒20 C	SNI
					PAGE	4 OF	10
	DQO	DOi	pos	200			
VOL 1 VOH 2 VOH 2	80,0MV 85.0MV 4.88 V 9.84 V	85.0MV 95.0MV 4.88 V 9.84 V	95'.0MY 110,MV 4,88 V 9,83 V	95.0MV 105.MV 4.89 V 9.84 V			
ION1	AME8.8 AMD.55 AMDE.5- AMT9.7-	8.40MA 19.8MA -3,35MA -7.37MA	7.70MA 17.1MA =3.28MA =7.06MA	7,95MA 17,9MA 53,35MA 47,41MA			
1021 1022 1023 1024	4.20NA 7.40NA 1.90NA 800.PA	6,00NA 2,60NA 6,60NA 8,10NA	2.30NA 5.60NA 2.20NA 300.PA	6,20NA 2,80NA 5,70NA 8,30NA			
1025 1026 1027 1028	7.60NA 7.90NA 7.70NA 7.90NA	1,50NA 1,40NA 1,40NA 1,40NA	7.80NA 7.50NA 7,70NA 7.40NA	1,40NA 1,20NA 1,30NA 1,40NA			
ILDP	#50,0UA						
IL1 IL2 IL3 IL4	⇔5,00UA ⇔5,00UA ⇔5,00UA						

RÇA	CDP1822SD	256 X 4	CMOS	STATIC	RAM	31	AUG	78	ŤEMP!	-55	C	SNI	12
									PAGE	5 6	ትም 1	rx.	

PASSED	GALPAT	(WIDE	LIMITSI	VCC=1ØV
PASSED	GALPAT	(TIGHT	LIMITS)	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS	VCC≈5V

PAGGEU	DATA RETENTIO	N TEST			
		VC	C = 4.5V	5 . 0v	10.0v
	S ACCESS TIME	CTAAD	220 N	175',N	65.0N
	ETUP TIME OLD TIME	(TDS) (TDH)	30 ON	22.ØN	8 80N
DAIM U	ofo traf	(nu)	8,00N	8_00N	10.0N
	S SETUP TIME	(TAS1)	12,0N	a, ppn	4.00N
	S SETUP TIME	(TAS2)	104 N	.84 gn	34.0N
	S HOLD TIME PULSE WIDTH	(TAH) (TWP)	+14 ØN 76 ØN	#12.0N	≂2.00N
MUTT	in#å∉ Atulu	(inc)	10.00	62.0N	30,0N
	ETUP TIME	(TCSS1)	142 N	120,N	54, ØN
	ETUP TIME	(TCSS2)	178 N	146.N	66,0N
	OLD TIME OLD TIME	(TCSH1) (TCSH2)	46 @N	38.0N	55,0N
40% II	ONO LINE	(icane)	ଡ•ପଡ	0.00	0.50
	ACTIVE FROM C		210.N	168, N	80 0N
	ACTIVE FROM C		238 N	145*N	56,ØN
սկեւնե	ACTIVE FROM ME	RD (TDOAS)	38 ØN	34.0N	50.0N
OUTPUT	HOLD FROM CS1	(TDOH1)	126 N	96. PN	26,0N
TUPTUO	HOLD FROM CS2	(TDOH2)	178 N	148 N	44, 0N
	HOLD FROM MRD	(TDOH3)	135 N	148 N 110 N	86,0N
	HOLD FROM MWR	(TPDH)	130 N	196,N	26.0N
	YCLE TIME CYCLE TIME	(TRC) (TWC)	216.N	176 N	104.N
MIX TO	6166	LIMCI	208 N	184.N	96.0N
	IIL	IIH	VICI	AICS	
AØ	=100.PA	100 PA	3,10 V	⊕3,08 V	
A1	9100.PA	200,PA	3.11 V	#3,11 V	
45	-100.PA	100,PA	3,13 V	ADPED A	
A3	-100.P∧	100 PA	3,13 V	-3.14 V	
A 4	#100 PA	100 PA	3.16 V	#3,14 V	
A5	-100.PA	100 _e PA	3,04 V	-3,14 V -3,10 V	
A 6	#100 PA	100.PA	3,04 V	#5 ₀ 11 V	
A7	~300.PA	100.PA	3.05 V	=3.Ø8 V	
CS1	e100.PA	100 PA	3.11 V	-3,10 V	
csa	-200.PA	100,PA	4,97 V	•4,95 V	
MWR	9100.PA	100,PA	4,97 V 3,08 V	۷ 90م5⊷	
MRD	-100.PA	100.PA	3.10 V	-3.Ø7 V	
010	#100.FA	100,PA	3.16 V	#3,10 V #3,10 V #3,11 V	
DII	-100.PA	100,PA	3,13 V	-3,10 V	
DIS	-100 PA	100,PA	3,15 V	#3,11 V	
DIB	m100.PA	100.PA	3.13 V	-3.08 V	

RCA	CDP1822SD	256 X 4 CMOS	STATIC RAM	51 AUG 78	TEMP	=55 C	SN:	12
					PÄGE	6 OF	10	
	מסמ	001	šoa	003				

	מסמ	001	Řod	003
VOL1 VOL2 VOL1	75',0MV 75.0MV 4.90 V 9.85 V	80.0MV 85.0MV 4,90 V 9.85 V	85,0MV 100,MV 4,89 V 9,85 V	85 # 0MV 95 # 0MV 4/90 V 9 # 86 V
IDN1 IDN1 IDP1	9.60MA 24.3MA -3.80MA -8.36MA	9,15MA 22,1MA -3,86MA -6,48MA	8.40MA AMS,191 AMS,158 AMS1.88	AMDT 8 AMD 25 AMDE 15 AMD 28
1071 1072 1073 1074	1.50NA 4.90NA =400.PA =1.20NA	3.20NA -200.PA 4.40NA 5.50NA	400.PA 3.80NA -200.PA -2.00NA	3.89NA 300.PA 2.90NA 5.50NA
1025 1026 1027 1028	5.50NA 5.30NA 5.50NA 5.20NA	-1,50NA -1,30NA -1,50NA -1,30NA	5,20NA 5,20NA 5,20NA 5,30NA	91,50NA 91,70NA 91,60NA 91,70NA
ILDP	⇒5°50∩V			
IL1 IL2 IL3 IL4	AU00,5= AU00,5= AU00,5= AU00,5=			

RCA CDP18288D 256)	4 CHOS STA	YTC RAH SI	AUG 78 TEMPÎ	85 C SÑI
•		•	PÄGE	Y OF 10
PASSED GALPAT (WIDE PASSED GALPAT (TIGHT PASSED GALPAT (TIGHT	LIMITS) VO	C=10V C=10V C=5V	REPRODUCIBILITY ORIGINAL PAGE	OF THE IS POOR
PASSED DATA RETENTION	TEST			
	VCC	a 4.Sy	ភ [*] ្ø∨	10.00
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	CAAT) CROT) CHOT)	217.N 24.6N 12.6N	165°N 16.0N 12.0N	85.0N 8.00N 14.0N
ADDRESS SETUP TIME ADDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WIOTH	(TAS1) (TAS2) (TAH) (TWF)	8.00N 108.N +14.0N 76.0N	5.00N 96.0N =12.0N 66.0N	4 . 00N 48 . 00N -2 . 00N 38 . 0N
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TC\$\$\bar{1}) (TC\$\$\bar{2}) (TC\$H1) (TC\$H2)	159 N 159 N 46 P ON 50 P ON	134, N 132, N 42, ON 46, NN	70,6N 68,0N 28,0N 26.0N
OUTPUT ACTIVE PROM CS OUTPUT ACTIVE FROM CS OUTPUT ACTIVE FROM ME	(SAOOT) S	212 m 219 m 48 m	156 N 154 N 42 M	94,2N 92,2N 26.0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH1) (TDOH2) (TDOH3) (TPOH) (TRC) (TWC)	146. 138. 138. 138. 138. 138. 138. 138.	110°N 110°N 110°N 110°N 190°N	32.00 32.00 30.00 30.00 30.00 30.00 30.00 30.00
IIL.	IIH	Vići	VICE	
			Tark of the	

	IIL.	IIH	VIĆ1	Aics
A0 A1 A2 A3	#21,2NA #21,2NA #22,4NA #19.3NA	19.3NA 21.0NA 21.8NA 19.1NA	2.86 V 2.89 V 2.90 V	#2,84 V #2,87 V #2,90 V #2,91 V
A4 A5 A6 A7	919,6NA 921,3NA 919,5NA 922,1NA	20,5NA 20,0NA 19.9NA 20,3NA	2,91 V 2,79 V 2,80 V 2,80 V	#2,86 V #2,86 V #2,85 V
CS1 CS2 MWR MRD	⇔20,1NA ⇔21,4NA ⇔20,6NA ⇔19.1NA	20,2NA 19,6NA 19,2NA 19,1NA	2,86 V 2,89 V 2,83 V 2,84 V	#2,85 V #2,89 V #2,84 V
010 011 012 013	=19,9NA =20,9NA =19,3NA =20.0NA	19,7NA 20.5NA 19.6NA 19.7NA	2.91 V 2.91 V 2.91 V	72,86 V 72,86 V 72,86 V

RCA	CDP1822SD	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMPi	85 C SNI	12
					PAGE	8 OF 10	
	000	100	sod	003			
A0F3 A0F3 A0F3	4.84 V	115, MV 130, MV 4,84 V 9,76 V	125.MV 155.MV 4.83 V 9.75 V	120, MV 145, MV 4,84 V 9,77 V			
IDN1 IDN2 IDP1 IDP2	-2.39MA	6.50MA 14.8MA -2,38MA -5.25MA	5.90MA 12.5MA #2.34MA #5.08MA	6,15MA 13,3MA m2,41MA m5,37MA			
1021 1022 1023 1024	189.NA	193, NA 196, NA 192, NA 199, NA	174,NA 169,NA <u>1</u> 71,NA 169,NA	189 NA 187 NA 191 NA 186 NA			
1025 1026 1027 1028	184.NA 194.NA	199, NA 197, NA 188, NA 200, NA	172 NA 177 NA 179 NA 170 NA	193, NA 178, NA 185, NA 188, NA			
ILDP	-5.00UA						
IL1 IL2 IL3 IL4	-20,0UA -25,0UA -25,0UA -20,0UA						

RCA	CDP1822SD	256 X 4	CHOS STATIC	RAM 31	AUG 78	TEMPE	125 C SN:	12
						0 x 0 E	8 80 (B	

PASSED	GALPAT	(WIDE	LIMITS)	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITSI	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS	VCC=5V

	VCC = 4.5V	5'øv	10°.00
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA) 220.N (TDS) 22.0N (TDH) 14.0N	195.N 18.dn 14.dn	95.0N 8.90N 14.0N
ADDRESS SETUP TIME ADDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WIDTH	(TAS1) 6,00N (TAS2) 114,N (TAH) -14,0N (TWP) 78,0N	6.09N 104.N =12.0N 70.0N	4.00N 56.0N -4.00N 42.0N
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS1) 160.N (TCSS2) 156.N (TCSH1) 50.0N (TCSH2) 54.0N	142°N 138°N 46°N 46°DN	76,0N 74,0N 28,0N 28,0N
OUTPUT ACTIVE FROM CS1 OUTPUT ACTIVE FROM CS2 OUTPUT ACTIVE FROM MRD	R (SAOOT) S	198, N 196. N 46. ØN	104.N 102.N 28.0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH1) 142.N (TDOH2) 138.N (TDOH3) 136.N (TPOH) 134.N (TRC) 248.N (TWC) 224.N	112'N 116'N 112'N 216'N	34,0N 34,0N 32,0N 32,0N 128,N 128,N
IIL	IIH VICE	vice	**
A1 =118.NA 1 A2 =121.NA 1	112,NA 2.84 V 113,NA 2.83 V 115,NA 2.88 V 111.NA 2.88 V	=2,81 V =2,84 V =2,88 V =2,88 V	
A5 #118.NA 1 A6 #115.NA 1	111,NA 2.89 V 111,NA 2.77 V 112,NA 2.77 V 112,NA 2.77 V	72,88 V 72,84 V 72,83 V 72,79 V	
CS2 w114.NA 1 MWR w115.NA 1	08,NA 2.87 V 09.NA 2.87 V 08.NA 2.79 V 2.80 V	-2,62 V -2,87 V -2,80 V -2,79 V	
DI2 =110 NA 1	09,NA 2.89 V 13.NA 2.86 V 09,NA 2.88 V 08,NA 2.86 V	=2,83 V =2,84 V =2,84 V =2,81 V	

RCA	CDP18228D	256 X 4 CMOS	STATIC RAM	31 AUG 78	工程列序 3	125 G SN1	12
					PAGE	18 OF 18	
	DOM	D01	pos	003			
VOL1	120.MV	125° MV	140 MY	135, MV 165, MV 4, B3 V 9, 73 V			
AOFS	130.MV	145.MV	170,MY	165 MY			
VOH	4.82 V	4,82 V	4.82 V	4 88 V			
VOHE	9,73 V	9.73 V	9.72 V	9',73 V			
IDNI	6,25MA	5.85MA	5 . 35MA	5,55MA			
IDNE	14.7MA	13,2MA	11,3MA	11.8MA			
IDP1	-2.15MA	-2.15MA	#2,12MA	AM8.11. AMP1,5			
1002	-4.71MA	-4.75MA	#4,54MA	#4.81MA			
1071	730.NA	730,NA	667.NA	675 NA			
Ioza	721.NA	717, NA	668,NA	678, NA			
1023	708.NA	717 NA	661.NA	673, NA			
IGZ4	716.NA	711.NA	662 NA	676.NA			
1025	722.NA	724.NA	679.NA	693, NA 692, NA 678, NA			
IDZ6	723.NA	730,NA	658 NA	692 NA			
IUZ7	710.NA	725,NA	662.NA	678 NA			
1028	717.NA	716.NA	664.NA	684.NA			
- -							

ILOP

IL1 IL2 IL3 IL4 ⇔5,00UA

#85,0UA #110.UA #85,0UA #75.0UA

RCA	CDP182280	256 X 4	CMOS	STATIC RAM	31	AUG 78	TEMP:	25 C	SN:	13
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PAGE 1 OF 10

PASSED GALPAT (TIGHT	LIMITS) VC	C=10V C=10V C=5V	REPRODUCIBILIT ORIGINAL PAGE	
PASSED DATA RETENTION	TEST			
	vcc	= 4.5V	5'.ØV	10,00
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA) (TDS) (TDH)	245.N 20,0N 12.0N	205'.N 16.9N 12.0N	80,0N 8,00N 8,00N
ADDRESS SETUP TIME ADDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WINTH	(TAS1) (TAS2) (TAH) (GWT)	12.0N 114.N -18.0N 64.0M	10,00 94,00 #12,00 56,00	4.00N 44.0N +2.00N 34.0N
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS1) (TCSS2) (TCSH1) (TCSH2)	148 N 144 N 38 P O N 42 P O N	128 N 126 N 126 N 34 M 38 M	22.0N 22.0N 22.0N 22.0N
OUTPUT ACTIVE FROM COUTPUT ACTIVE FROM COUTPUT ACTIVE FROM ME	(SACOT) SE	232.N 230.N 50.0N	196 N 192 N 44 M	86 0N 86 0N 88 0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH1) (TDOH2) (TDOH3) (TPOH) (TRC) (TWC)	148.N 146.N 140.N 136.N 256.N	118, N 114, N 118, N 112, N 216, N	34,0N 34,0N 30,0N 30,0N 112.N
TIL	IIH	VICI	VTC2	
A0 -2.80NA A1 -3.10NA A2 -3.00NA A3 -2.70NA	3,20NA 2,70NA 2,40NA 3.00NA	2.90 V 2.94 V 3.02 V 2.99 V	#2,99 V #3,01 V #2,99 V	
A4 =6.00NA A5 =3,10NA A6 =2,40NA A7 =2,40NA	2,40NA 2.80NA 2.70NA 2.40NA	3.04 V 2.90 V 2.93 V 2.93 V	=3,06 V =2,93 V =2,97 V =2,96 V	
CS1 =2.50NA CS2 =2.70NA MWR =2.10NA MRD =2.60NA	2,70NA 2,50NA 2,70NA 2.50NA	3.00 V 3.04 V 2.99 V 2.99 V	=2,99 V =3,03 V =2,98 V =3,00 V	
DIO =2,60NA DI1 =3,30NA DI2 =3,40NA DI3 =3,20NA	3.00NA 3,00NA 4.40NA 2.50NA	3.05 V 3.03 V 3.11 V 3.08 V	=2,99 V =2,99 V =3,06 V =3,04 V	
		B-121		

RCA	CDP1822SD	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP
		No. of the second second			PAGE
	DOM	001	noa	003	
AOH 7 AOH 7 AOT 5 AOT 7	110.MV 110.MV 4.85 V 9.79 V	110, MV 120, MV 4, 85 V 9,79 V	125.MV 140.MV 4.84 V 9.77 V	120 MV 135 MV 4,84 V 9,78 V	
IDN1 IDN2 IDP1 IDP2	6.70MA 17.0MA =2.56MA =5.78MA	6',55MA 16.0MA -2,57MA -5.81MA	5',95MA 13'8MA -2,49MA -5.61MA	6,00MA 14.2MA 2.53MA 5,77MA	
10Z\$ 10Z2 10Z3 10Z4	14,5NA 15,2NA 8,00NA 10,4NA	9'.30NA 7'.40NA 14,5NA 12.3NA	13',5NA 15',6NA 8,40NA 9,20NA	11.3NA 8.40NA 15,3NA 13.9NA	
1025 1026 1027 1028	13,5NA 13,1NA 13,2NA 13.1NA	8,10na 8,30na 8,00na 8.30na	14,1NA 14,5NA 14,5NA 14,3NA	8,60NA 8,40NA 8,50NA 8,50NA	
ILDP	-5. 00U∧				
IL1 IL2 IL3 IL4	₩10,0UA ₩10,0UA ₩175.UA ₩175.UA				

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PASSED	GALPAT	CMIDE	LIMITS)	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS)	VCC=10V
PASSED	GALPAT	CTIGHT	LIMITS)	VCC=5V

PASSED DATA RETENTION TEST

			_*	i mt m
	VCC	= 4 _* 5V	5 . øv	10.0V
ADDRESS ACCESS TIME	(TAA)	250.N	200°N	75.0N
DATA SETUP TIME	(TDS)	24.0N	18,0N	6.90N
DATA HOLD TIME	(TDH)	10.0N	10,0N	10.0N
ADDRESS SETUP TIME	(TAS1)	16.0N	12.0N	4 . 00N
ADDRESS SETUP TIME ADDRESS HOLD TIME	(SSAT) (Hat)	114.N	92.ØN #12.ØN	40,0N +2.00N
WRITE PULSE WIDTH	(TWP)	#18 ØN 70 øN	65*WN	32,0N
CS: SETUP TIME	(TC9S1) (TCSS2)	146,N 142,N	124, N 120. N	60,0N 58,0N
CS1 HOLD TIME	(TCSH1)	36,0N	30 N	22,0N
CS2 HOLD TIME	(TCSH2)	38 ØN	32,0N	50,0N
OUTPUT ACTIVE FROM CS	1 (TDOAT)	238.N	192,N	82,00
OUTPUT ACTIVE FROM CS		234.N	190 N	80,0N
OUTPUT ACTIVE FROM MR	D (TDOA3)	48. QN	42.0N	55.0N
OUTPUT HOLD FROM CS1	(100H1)	142 N	110, N	32, ON
DUTPUT HOLD FROM CS2	(TDOH2)	138.W	108 N	32,0N
OUTPUT HOLD FROM MRO	(TDDH3)	138.N	116 N	28,0N
OUTPUT HOLD FROM MWR READ CYCLE TIME	(TPDH) (TRC)	134.N 232.N	110,N 200,N	96,0N
WRITE CYCLE TIME	CTWC	N.SES	184.N	96.0N
IIL	IIH	VICI	AICS	
AØ 9400,PA	800 PA	3.00 V	-3.00 V	
A1 #600,PA	400, PA	3,04 V	-3,03 V	
	400,PA	3.13 V	+3.10 V +3.09 V	
AS TOWNSPA	700.PA	3.99 V	m J _a Vy V	
_	400.PA	3,13 V	#3,15 V	
	500.PA	3.00 V	3.04 V	
A6 ∞400°PA '	500,PA 400.PA	3.03 V 3.03 V	=3,07 V =3,06 V	
CS1 =400.PA :: CS2 =500.PA ::	500, PA	3.11 V 3.14 V	93,09 V 93,12 V 93,08 V	
MWR =300.PA	400 PA 400 PA	3,09 V	*3.08 V	
MRD #400.PA	500 PA	3.10 V	=3.10 V	
DI0 -400.PA	400, PA	3.15 V	-3,09 V	
DII #800 _s PA	600 _e PA	3,14 V	-3,09 V	
DI2 @700,PA	900,PA	3,20 V	-3,15 V	
DI3 #800.PA	500.PA	3.17 V	#3.13 V	

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RCA	CDP18228D	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP
					PAGE
	DQØ	001	DOS	003	
AOH5 AOH7 AOF3 AOF1	109.MV 95.0MV 4.88 V 9.82 V	100,MV 105,MV 4,80 V 9,82 V	110.MY 120.MV 4.87 V 9.81 V	110 MV 115 MV 4,87 V 9,81 V	
IDN1 IDN2 IDP1 IOP2	7.40MA 19.3MA +3.01MA +6.78MA	7.25MA 18.2MA ⇔3.03MA ⇔6.86MA	6.60MA 15.8MA #2.96MA #6.59MA	6170MA 16.2MA -2.98MA -6.78MA	
1021 1022 1023 1024	2.00NA 500.PA 7.50NA 4.80NA	5.40NA 7.00NA ⇒300.PA 1.40NA	2.50NA 300.PA 7.60NA 5.40NA	4,50NA 7,60NA 600.PA 1.50NA	
1025 1026 1027 1028	1.80NA 2.10NA 1.70NA 1.90NA	5,10NA 5,30NA 5,20NA 5,30NA	1.30NA 900.PA 1.10NA 900.PA	6.90NA 6,40NA 6,60NA 6.30NA	
ILDP	⇔5.00UA				
IL1 IL2 IL3 IL4	AUNN,E⇔ AUNN,E⇔ AU,RNS⇔ AU,RNS⇔				

SNS

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PAGE 5 OF 10

PASSED	GALPAT	(WIDE	LIMITS)	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS)	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS)	VCC*5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

	VCC	= 4,5V	5.0v	10'.0v
ADDRESS ACCESS TIME	(AAT)	250 N	190'N	70,0N
DATA SETUP TIME	(Bdt)	30' 0N	22'0N	8.00N
DATA HOLD TIME	(Hdt)	8 00N	8'00N	10.0N
ADDRESS SETUP TIME	(TAS1)	16.04	19,0N	4.00N
ADDRESS SETUP TIME	(TAS2)	112.N	_90,0N	36.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	~12,0N	-2.00N
WRITE PULSE WIDTH	(TWP)	68.0N	62.0N	30.0N
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS1)	150 N	122', N	56,0N
	(TCSS2)	148 N	120', N	54,0N
	(TCSH1)	42 DN	34', ON	20,0N
	(TCSH2)	46 DN	36', ON	18.0N
OUTPUT ACTIVE FROM CS	(SADOT) SE	246.N	192, N	80,0N
OUTPUT ACTIVE FROM CS		242.N	190, N	78,0N
OUTPUT ACTIVE FROM MR		44.ØN	38, AN	22.0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH1) (TDOH2) (TDOH3) (TPOH) (TRC) (TWC)	138.N 134.N 136.N 132.N 224.N	106, N 104, N 114, N 110, N 200, N 176, N	32,0N 32,0N 28,0N 28,0N 104,N 96.0N
IIL	IIH	VIC1	VICE	
A0 *100,PA	300 PA	3,12 V	#3,11 V	
A1 *100,PA	100 PA	3,15 V	#3,14 V	
A2 *100,PA	100 PA	3,22 V	#3,29 V	
A3 *100,PA	200 PA	3,29 V	#3,18 V	
A4 ~400.PA A5 ~100.PA A6 ~100.PA A7 ~100.PA	100.PA 100.PA 100.PA	3.23 V 3.12 V 3.14 V 3.13 V	-3,24 V -3,15 V -3,18 V -3,17 V	
CS1 =100.PA	100 PA	3.21 V	23,19 V	
CS2 +100.PA	100 PA	3.24 V	23,22 V	
MWR =100.PA	100 PA	3.18 V	23,17 V	
MRD =100.PA	200 PA	3.19 V	23,19 V	
DIO =100.PA	100.PA	3,26 V	#3,19 V	
DI1 =200.PA	200.PA	3,25 V	#3,19 V	
DI2 =200.PA	200.PA	3,30 V	#3,25 V	
DI3 =300.PA	100.PA	3,28 V	#3,23 V	

RCA	CDP18225D	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP:	₹55 C	SNI
					PĀGE	6 OF 1	Ø
	DOØ	100	soa	500			
VOL1 VOL2 VOH1	95,0MV 90,0MV 4.89 V 9.84 V	95,0MV 95,0MV 4,89 V 9,84 V	105.MV 110.MV 4.88 V 9.84 V	105 MV 105 MV 4 88 V 9 84 V			
IDN1 IDN2 IDP1 IDP2	7.95MA 21.2MA -3.44MA -7.78MA	7.85MA 20.1MA -3,49MA -7.87MA	7.15MA 17.5MA -3.40MA -7.61MA	7,20MA ,17,9MA ,3,43MA ,7,82MA			
10Z1 10Z2 10Z3 10Z4	3.50NA 5.90NA -1.20NA -100.PA	1,20NA -1,50NA 5,60NA 4,10NA	2,20NA 5.70NA 41.20NA ANQ1.1#	2,40NA -1,00NA 4,60NA 4,70NA			
1025 1026 1027 1028	4.50NA 4.30NA 4.40NA 4.20NA	-1,50NA -1,20NA -1,40NA -1,20NA	4.80NA 4.80NA 4.60NA 4.70NA	#1,40NA #1,50NA #1,50NA #1,50NA			
ILDP	≈5 . 00U∧			•			
IL1 IL2 IL3 IL4	=5.00U4 +5.00UA =230,1A =230.UA						

PASSED GALPAT (WIDE LIMITS) VCC=10V PASSED GALPAT (TIGHT LIMITS) VCC=10V PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

ļ:

	vac	= 4.5V	5 . 0v	10.0V
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA) (TDS) (TDH)	235.N 20,0N 14.0N	200.N 16.0N 14.0N	90.0N 8.00N 14.0N
ADDRESS SETUP TIME ADDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WINTH	(TAS1) (TAS2) (TAH) (TWT)	8.00N 110,N +16,0N 74.0N	8.00N 96.0N =12.0N 66.0N	4.00 -2.00 -2.00 -3.00 -3.00
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLO TIME CS2 HOLD TIME	(TCSS1) (TCSS2) (TCSH1) (TCSH2)	156 N 150 N 44 ON 48 ON	134 ² N 130 ² N 40.0N 42.0N	70,0N 68,0N 26,0N 26.0N
OUTPUT ACTIVE FROM CS OUTPUT ACTIVE FROM MR	(SADOT) S	230.N 224.N 52.0N	198, N 194, N 46, AN	98,0N 96,0N 88.0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH1) (TDOH2) (TDOH3) (TPOH) (TRC) (TWC)	150.N 146.N 140.N 134.N 256.N 224.N	120, N 118, N 118, N 112, N 224, N 200, N	38,0N 38,0N 38,0N 120.N 120.N
III.	IIH	VICI	AICS	
A1 =34,8NA A2 =37,0NA	35,4NA - 34,2NA 33,7NA 36,6NA	2.85 V 2.89 V 2.97 V 2.94 V	-2.85 V -2.88 V -2.96 V -2.94 V	
A5 #36.2NA A6 #34.2NA	33,9NA 34,4NA 34,8NA 33,7NA	2.99 V 2.85 V 2.88 V 2.88 V	-3.02 V -2.88 V -2.91 V -2.91 V	
CS2 -34,7NA	35,2NA 35,6NA 35,4NA 34,7NA	2,95 V 2,99 V 2,94 V 2,94 V	#2,94 V #2,99 V #2,94 V #2,95 V	
DIO =33.2NA DI1 =35.1NA DI2 =34.2NA DI3 =34.2NA	34,8NA 36,5NA 40,0NA 34,2NA	3,00 V 2,98 V 3,06 V 3,03 V	-2,94 V -2,93 V -3,99 V	

RCA	CDP1882SD	256	X	4	CMOS	STATIC	RAM	31	AUG	78	TEMP:	85	¢	SN:	13
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	noø	001	boa	003	
VOL 1	125.MV	130.MV	145.MV	140° MV	
V01.2	130 MV	140.MV	165.MV	160.MV	
VOH:	4.82 V	4,82 V	4.82 V	4,82 V	
SHOV	9.74 V	9.75 V	9.73 V	9.74 V	
IDN1	5.85MA	5.70MA	5.15MA	5 <u>.</u> 25MA	
ZNOI	14.6MA	13,6MA	11,7MA	12,1MA	
IOP1	-2.16MA	-2,18MA	⊕2.11MA	+2,13MA	
1065	-4.93MA	≈4.95MA	#4.71MA	=4.92MA	
IUZ1	-32,7NA	-39,4NA	#33 1NA	-35,2NA	
1072	=41.6NA	-39.9NA	-39,6NA	-34.1NA	
1023	₩40.8NA	-47,8NA	-39,6NA -38,2NA	-41.2NA	
IOZ4	⇒39,3 NA	-48.4NA	-38.1NA	-42.7NA	
1025	-46.9NA	-43.3NA	#46,1NA	#36,4NA	
1026	-47 4NA	-44,2NA	-44 9NA	-36,2NA	
1027	-48.6NA	-44.5NA	~47,2NA	+37,9NA	
1028	-47.3NA	-45,1NA	=44 3NA	#38.1NA	
ILDP	8.20UA				
ILi	-40.0UA				
IL2	⇔50≟0UA				
IL3	≈170,IJΛ				
IL4	#165.UA				

PAGE 9 0F 10

	LIMITS) V	CC=10V CC=5V	REPRODUCIBILITY ORIGINAL PAGE IS	OF THE POOR
PASSED DATA RETENTION	I TEST			
	vc	C = 4,5V	5 '. 0v	10'.CV
AUDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA) (TDS) (TDH)	245.N 20,0N 14.0N	215*N 16.0N 14.0N	95.ØN 8.ØØN 14.ØN
ADDRESS SETUP TIME ADDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WINTH	(TAS1) (TAS2) (TAH) (TWP)	4.00N 118.N -14.0N 76.0N	4 MAN 104 N -12 AN 68.0N	4.00N 56.0N 4.00N 42.0N
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS1) (TCSS2) (TCSH1) (TCSH2)	154.N 46,0N	138, N 136, N 42, AN 44, AN	74,0N 72,0N 28,0N 26.0N
OUTPUT ACTIVE FROM CS OUTPUT ACTIVE FROM CS OUTPUT ACTIVE FROM MR	(SADOT) S	244.N	216, N 214, N 50, ON	106.N 106.N 30.0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH1) (TDOH2) (TDOH3) (TPOH) (TRC) (TWC)	146.N	120'N 116'N 118'N 114'N 232'N 200'N	40,0N 40,0N 36,0N 120,N 128,N
IIL	ITH	VIC1	AICS	
A0 =202.NA A1 =199.NA A2 =209.NA A3 =203.NA	198.NA 193,NA 195.NA 201.NA	2.81 V 2.86 V 2.95 V	-2,81 V -2,85 V -2,94 V -2,92 V	
A4	194, NA 195, NA 197, NA 193. NA	2.97 V 2.81 V 2.84 V 2.84 V	#3,00 V #2,85 V #2,89 V #2.88 V	
CS1 =204.NA CS2 =201.NA MWR =198.NA MRD =204.NA	197.NA 203,NA 197.NA 196.NA	5.91 V 5.92 V 5.98 V	#2,93 V #2,97 V #2,91 V #2,93 V	
DID #192.NA DI1 #196.NA DI2 #196.NA DI3 #195.NA	198.NA 201.NA 206.NA 197.NA	2.97 V 2.95 V 3.04 V 3.00 V	=2,91 V =2,91 V =3,00 V =2,97 V	
		B-129		

RCA	CDP185580	256 X 4	4	CMDS	STATIC	RAM	31	AUG	78	TEMP	125	C	SN:	13
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PAGE 10 OF 10

	000	001	0.05	Dua
VOLI	140.MV	145, MV	160.MV	160, MV
VOLS	145.MV	155.MV	185.MV	175.MV
VOH	4.80 V	4,80 V	4.80 V	4,80 V
ADH5	9.72 V	9.72 V	9.70 V	9 72 V
TUNI	5.30MA	5.15MA	4.70MA	4.75MA
IDN2	13.0MA	AMS.SI	10.5MA	10.8MA
IDP1	-1,94MA	-1.99MA	- #1.91MA	=1.93MA
IUP2	-4.40MA	-4.47MA	-4.26MA	=4 39MA
TOZI	#613.1·A	-613 NA	=594.NA	-553, NA
1072	-637.NA	-616.NA	#602,NA	-566,NA
1023	-644.NA	-627,NA	-610.NA	-567, NA
IOZ4	#650.NA	-625 NA	-609.NA	-572 NA
1025	-643.NA	~625.NA	=611.NA	-575,NA
IUZ6	-656.NA	-645,NA	-607.NA	584 NA
1027	=644.NA	-643,NA	-606.NA	-575,NA
1078	-654,NA	-633 NA	-615.NA	-579 NA
ILDP	90 <u>.</u> 0UA			
	FE M M M M			
IL1	+180.UA			
ILS	=240.UA			
ÎĻ3	-270.UA			
IL4	-250.UA			
Wa Y	··· Carrigation			

PASSED GALPAT (WIDE LIMITS) VCC=10V PASSED GALPAT (TIGHT LIMITS) VCC=10V PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

	VCC	# 4.5V	5 ' .øv	10.0V
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA) (TOS) (TDH)	185.N 18,0N 10.0N	160'.N 16,0N 10,0N	75.ØN 8.ØØN 12.ØN
ADDRESS SETUP TIME ADDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WIDTH	(TAS1) (TAS2) (TAH) (TWP)	14,0N 96,0N +12,0N 54,0N	10.0N 84.0N +10.0N 50.0N	4.00H 42.0H -2.00H 32.0H
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS1) (TCSS2) (TCSH1) (TCSH2)	128 N 126 N 32 ON 34 ON	112,N 110.N 30.0N 30.0N	50,0N 58,0N 60,0N 0,0N
OUTPUT ACTIVE FROM CS OUTPUT ACTIVE FROM CS OUTPUT ACTIVE FROM MR	(SADOT) S	178 ₈ N 176 ₈ N 40 a Ø N	156 N 154 N 36.0N	82,0N 80,0N 80,0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH1) (TDOH2) (TDOH3) (TPOH) (TRC) (TWC)	124.N 122.N 130.N 126.N 200.N	94.0N 94.0N 110.N 104.N 176.N 160.N	22,0N 22,0N 28,0N 28,0N 104,N
TIL	IIH	VICI	AICS	
A1 #1.60NA A2 #1.00NA	1.10NA 800.PA 1.00NA 1.20NA	2.61 V 2.63 V 2.64 V 2.63 V	#2,59 V #2,65 V #2,68 V #2,67 V	
A5 =1.20NA A6 =1.10NA	3,40NA 1,20NA 1,30NA 1,10NA	2.63 V 2.58 V 2.61 V 2.60 V	#2,64 V #2,64 V #2,64 V	
CS2 -1,00NA MWR -1.20NA	1,10NA 1.30NA 900.PA 1.10NA	2.62 V 2,64 V 2.59 V 2.60 V	~2,63 V ~2,64 V ~2,61 V ~2,62 V	
DI1 #1,00NA DI2 #1,30NA	1.10na 1.30na 1.00na 1.00na	2.69 V 2.67 V 2.70 V 2.67 V	#2,65 V #2,63 V #2,66 V #2,64 V	

RCA	CDP18225D	256 X 4 CMOS	STATIC RAM	31 AUG 78 TEMP:	25 C	SN:	14
				PAGE	a of	10	:
	000	DO:	noa	003			;
VOL 1	85.0MV 95.0MV	90 @MV 105 MV	95',0MV 120.MV	95.0MV 115.MV			:

		·		
VOH1	4.87 V	4.87 V	4,86 V	4.86 V
SHOV	9.80 V	9.80 V	9 80 V	9.80 V
IDNi	8.70MA	AMRE.B	7.65MA	7.85MA
IDNS	20.1MA	18.3MA	15'_8MA	16,504
IDP1	-3.DOMA	-2,94MA	-2.89MA	-2,97MA
ippa	-6.30MA	-6.26MA	-6,03MA	46.33MA
IOZi	36. ONA	35,8NA	42'_3NA	35.6NA
Ioza	32.3NA	37.7NA	38,8NA	37,9NA
1023	33.0NA	37.9NA	37,7NA	40.1NA
IOZ4	36.1NA	34,2NA	40.6NA	37.9NA
1025	30,9NA	40.0NA	38,5NA	42.5NA
1026	31,8NA	41.2NA	38,5NA	41.2NA
1027	31.7NA	40.4NA	38,1NA	41.5NA
IOZ8	31.1NA	40.3NA	37.8NA	40.5NA

ILDP -5.00UA IL1 IL2 IL3 IL4

-15.0UA -25.0UA -50.0UA

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PASSED	GALPAT	(WIDE	LIMITS)	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS)	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS)	VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

	vcc	= 4,5V	5.0V	10.0V
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA)	185.N	155'N	65'.0N
	(TDS)	20.0N	16.0N	6.00N
	(TDH)	8.00N	8.09N	10.0N
ADDRESS SETUP TIME	(TAS1)	14,0N	10.AN	4.00N
ADDRESS SETUP TIME	(TAS2)	88,0N	74,AN	36.0N
ADDRESS HOLD TIME	(TAH)	~10,0N	-10.AN	-2.00N
WRITE PULSE WIDTH	(TWP)	56.0N	50.AN	30.0N
CS1 SETUP TIME CS2 SETUF TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS1)	122.N	104, N	54,0N
	(TCSS2)	120.N	102, N	52,0N
	(TCSH1)	30.0N	28, ON	20,0N
	(TCSH2)	32.0N	30. ON	18.0N
OUTPUT ACTIVE FROM CS	(SAOQT) S	168.N	144, N	00,00
OUTPUT ACTIVE FROM CS		166.N	142. N	78,00
OUTPUT ACTIVE FROM MR		36.ON	32. MN	22.00
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH1) (TDOH2) (TDOH3) (TPOH) (TRC) (TWC)	116.N 116.N 128.N 124.N 192.N 176.N	88.0% 86.9N 108,0 104,0 168,0 144.0	20
IIL	IIH	VICI	AICS	
A0 =200,PA	200.PA	2.75 V	22,73 V	
A1 =300,PA	100.PA	2.77 V	22,79 V	
A2 =200.PA	100.PA	2.78 V	22,81 V	
A3 =300.PA	300.PA	2.76 V	22,81 V	
A4 #200.PA	1.40NA	2.77 V	#2,78 V	
A5 #200.PA	200.PA	2.71 V	#2,76 V	
A6 #200.PA	300.PA	2.74 V	#2,77 V	
A7 #200.PA	200.PA	2.73 V	#2,78 V	
CS1 =200.PA	200.PA	2.75 V	-2,76 V	
CS2 =200.PA	200.PA	2.78 V	-2,77 V	
MWR =200.PA	100.PA	2.73 V	-2,75 V	
MRD =200.PA	200.PA	2.74 V	-2,75 V	
DIO =200.PA	200.PA	2.83 V	=2,78 V	
PA =200.PA	300.PA	2.81 V	=2,76 V	
DI2 =200.PA	200.PA	2.84 V	=2,79 V	
DI3 =200.PA	200.PA	2.80 V	=2,77 V	

RCA COP1822SD 256 X 4 CMOS STATIC RAM 31 AUG 78 TEMP: -20 C SN: 14

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	non	001	005	503
VOH2	75.0MV 80.0MV 4.89 V 9.84 V	75.0MV 90.0MV 4.89 V 9.84 V	85'.0MV 100.MV 4.89 V 9.83 V	80.0MV 95.0MV 4,89 V 9.84 V
ION1 IDN2 IDP1 IUP2	10,0MA 23,4MA =3,56MA =7,43MA	9.65MA 21.4MA -3.53MA -7.39MA	8.85MA 18.6MA #3.44MA #7.15MA	9.10MA 19.3MA -3,55MA -7.49MA
1021 1022 1023 1024	7.70NA 6.50NA 1.10NA 4.10NA	1,90NA 1,10NA 7,40NA 4,50NA	6_80NA 7_50NA 600_PA 3_10NA	2,50NA 800,PA 7,80NA 5,30NA
1025 1076 1027 1028	4.50NA 4.50NA 4.80NA 4.60NA	2.80NA 3.20NA 2.70NA 3.10NA	5,60NA 5.80NA 5.60NA 5.80NA	2,59NA 2,29NA 4NR2.5
ILDP	⇔5.00UA			
IL1 IL2 IL3 IL4	-10.0UA -20.0UA -40.0UA -35.0UA			

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PASSED	GALPAT	CWIDE	LIMITS	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS)	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITSI	VCC=5V

	VCC	= 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA) (TDS) (TDH)	175.N 22.0N 6.00N	140 N 16 N 8 NON	60'.0N 6.00N 10.0N
ADDRESS SETUP TIME ADDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WIDTH	(TAS1) (TAS2) (TAH) (TWP)	10.0N 84.0N -12.0N 50.0N	8.00N .70.0N #10.0N 44.0N	4.00N 32.0N ~2.00N 28.0N
esi setup time cs: setup time cs: hold time cs: hold time	(TCSS1) (TCSS2) (TCSH1) (TCSH2)	114.N 114.N 34.QN 34.QN	98,0N 96,0N 28,0N 28,0N	90,0N 48,0N 20,9N 18.0N
OUTPUT ACTIVE FROM CS1 OUTPUT ACTIVE FROM CS2 OUTPUT ACTIVE FROM MRC	(SADOT)	166.N 162.N 32.0N	136 N 134 N 30 MN	76.0N 74,0N 20.0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOM1) (TDOH2) (TDOH3) (TPOH) (TRC) (TWC)	110,N 110,N 126,N 124,N 184,N	82.0N 82.0N 108.N 102.N 144.N 136.N	20,000 24,000 24,000 24,000 88.00
IIL I	IIH	VIC1	VICE	
AE #100.PA (7,00 A 0,00 A 0,00 A 1,00 PA	2.85 V 2.88 V 2.88 V 2.87 V	#2,84 V #2,89 V #2,91 V	
A5 0.00 A 1 A6 0.00 A 1	300 PA 100 PA 100 PA 100 PA	2.88 V 2.83 V 2.85 V 2.84 V	#2.88 V #2.88 V #2.88 V	
CS2 0.00 A 1	100,PA 100.PA 1.00.A 100.PA	2,87 V 2.89 V 2.84 V 2.85 V	=2.87 V =2.88 V =2.85 V	
DI1 0,00 A 1	0.00 A 100.PA 2.00 A 3.00 A	2.93 V 2.92 V 2.94 V 2.91 V	#2,89 V #2,89 V #2,88 V	

RÇA	CDP1822SD	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP:	+55 C	SNI	14
					PAGE	6 OF	10	
	ngø	D01	son	003				
00H5 00H1 00H1	65,0MV 70,0MV 4,90 V 9,86 V	65.0MV 75.0MV 4.91 V 9.86 V	75,0MV 90,0MV 4,90 V 9,85 V	70,0MV 85,0MV 4,91 V 9,86 V				
IDN1 IDN2 IDP1 IDP2	11,3MA 26,5MA #4,11MA #8,56MA	10.8MA 24.3MA -4.13MA -8.70MA	10,0MA 21.3MA 44.06MA 48.34MA	10,2MA 27,0MA -4,17MA -8.73MA				
1021 1022 1023 1024	#1.00NA 400.PA 3.60NA #100.PA	5,90NA 3,50NA -1,00NA 2,70NA	-1.50NA -1.10NA 3.90NA 500.PA	5,10NA 4,00NA -1,30NA 2.00NA				
1025 1026 1027 1028	2.80NA 2.90NA 2.40NA 2.80NA	800.PA 1,00NA 1,10NA 1,20NA	1.70NA 1.20NA 1.50NA 1.20NA	1,80NA 1,80NA 2,00NA 1,90NA				
ILDP	≈5.00UA							
IL1 IL2 IL3 IL4	#10,0UA #20,0UA #30,0UA #35,0UA							

RCA	COP1822SD	256 X 4 CMD	S STATIC RAM	31 AUG 78	TEMP:	85 C	SN:	14
					PAGE	7 OF :	10	•
PASS	ED GALPAT ED GALPAT FD GALPAT	(WIDE LIMITS CTIGHT LIMITS) VCC=10V	REPRODU	CBILITY (OF THE		

PASSED DATA RETENTION TE	: e T		ORIGINAL PAGE	IS POOR
A WOOCD DATA KETER TON TE	201			
	VCC	= 4.5V	5 . 0v	10.0v
ADDRESS ACCESS TIME	(TAA)	190 N	170°N	80'.0N
DATA SETUP TIME	(TDS)	18, ØN	16.0N	8.00N
DATA HOLD TIME	(TDH)	10.0N	12.08	12.00
1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1	(10,11)	11181214		TERRIO
ADDRESS SETUP TIME	(TAS1)	10'.0N	8,000	4.00N
ADDRESS SETUP TIME	(TAS2)	iga.N	92.0N	48.0N
AUDRESS HOLD TIME	(HAT)	-14 ON	-10,0N	-5 40N
WRITE PULSE WINTH	(TWP)	64.0N	SA, AN	36,0N
Hurria Dear Manie	() ()	Odebu	23 (1 tg (/ L))	20 9 614
CS: SETUP TIME	(TCSSI)	134 N	118, N	64, 2N
CS2 SETUP TIME	(TCSS2)	132 N	116.N	65°0N
CS1 HOLD TIME	(TCSH1)	40,0N	38.0N	26.0N
CS2 HOLD TIME	(TCSH2)	42.0N	38.0N	26,0M 24,0N
An and San	(1 0 0 1 1 E)	4 C A D 1	"Srio Kila	Led [®] stire
OUTPUT ACTIVE FROM CS1	(TDOA1)	192.N	170, N	90,0N
OUTPUT ACTIVE FROM CS2	(SADOT)	190.N	168.N	96,0N
DUTPUT ACTIVE FROM MRD	(TDOA3)	44.0N	40.0N	26.0N
		•		
OUTPUT HOLD FRAM CS:	(TOOH1)	128_N	98. ØN	24, ØN
OUTPUT HOLD FROM CS2	(SHOOT)	126,N	96.ØN	24,0N
OUTPUT HOLD FROM MRD	(YD0H3)	132.N	112,N	HO, OF
OUTPUT HOLD FROM MAR	(TPDH)	128.N	106 N	30.0N
READ CYCLE TIME	(TRC)	216.N	192,N	120.N
WRITE CYCLE TIME	CTMC)	184.N	176.N	112.N
	11 1 1-12 g	1000	T & CO B IV	T + C # 14
IIL III	ł	VIC1	VTCP	
A0 -13,4NA 12,	ANP.	2,53 V	-2,51 V	
	SNA	2.56 V	≈2,58 V	
	3NA			
- 4		2,58 V 2,55 V	#2,61 V	
wa wideligh in	ANA	K.33 V	-2.61 V	
A4 913,3NA 18,	6NA	2'.56 V	÷2,58 V	
	4NA	2.5Ø V	ล์2 ็รร v	
	3NA	2.53 V	257 V	
	7 N A	5.55 V	-2,55 V -2,57 V -2,57 V	
ा सम्बद्धाः क्षेत्री ।	, - * F FT	1. g . l C. V		
	4NA	2.54 V	-a,55 v	
CS2 =13,0NA 14.	7NA	2,57 V	#2,58 V	
MWR =13,3NA 12.	5NA	2,51 V	÷2,54 v	
	ONA	2.52 V	-2.54 V	
		* =	~	

2,62 V 2,60 V 2,63 V 2,60 V #2,55 V #2,55 V #2,59 V

DIØ

013 013 =12.9NA =13.0NA =13.0NA =13.1NA 13.9NA 13.9NA 13.1NA 12.5NA

RCA	CDP1822SD	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP:	85 C S
					PAGE	8 OF 10
	000	D01	pas	D03		
VOL 1	100.MV	105, MV	115 MV	110° MV		
VUL 2	110 MV	125.MV	145 MV	135 MV		
VOH:	4.84 V	4.84 V	4.84 V	135 MV 4 84 V		
AOHS	9.76 V	9.76 V	9.76 V	9,77 V		
IDNI	7,30MA	7 . 00 M A	6.40MA	6.60MA		
IDNS	16.9MA	15.4MA	13.3MA	_13.9MA		
IDP1	42.52MA	-2.48MA	#2.39MA	-2,50MA		
IDP2	⇔5.31MA	-5.29MA	=5.96MA	-5.36MA		
TOZI	411.NA	463.NA	471.NA	458, NA		
IOZ2	4 73 B . N A	458.NA	477.NA	456 NA		
1073	404.NA	460,NA	473.NA	458,NA		
IOZ4	410.NA	454 NA	482.NA	460.NA		
1025	417,NA	472.NA	502.NA	486 NA		
IUZ6	435 NA	476 NA	494 a N A	495 NA		
IU27	418 NA	481.NA	485.NA	476, NA		
1028	420.NA	465.NA	494.NA	473.NA		
ILDP	⇔5.00⊞A					
11.1	→30.0 UA					
11.2	-45.PUA					
ILB	-75 aU∧					
IL4	=75.0UA					
d by "	Contraction Clark					

SN:

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PASSED	GALPAT	CMIDE	LIMITS)	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS)	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS)	VCC=5V

	VCC	= 4.5V	5'.øv	10°.00
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA) (TDS) (TDH)	205.N 20,0N 12.0N	180'N 16.0N 12.0N	90.0N 8.0N 14.0N
ADDRESS SETUP TIME ADDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WIDTH	(TAS1) (TAS2) (TAH) (TWP)	8.00N 110.N -14.0N 70.0N	8.00N 100'N -12.0N 62.0N	4.00n 56.0n -4.00n 38.0n
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS1) (TCSS2) (TCSH1) (TCSH2)	144.N 142.N 46.2N 46.2N	126.N 126.N 40.0N 42.0N	70,0N 68,0N 28,0N 26.0N
OUTPUT ACTIVE FROM CS OUTPUT ACTIVE FROM CS OUTPUT ACTIVE FROM MR	(SA00T) S	208.N 204.N 48.0N	184,N 182,N 42.0N	102.N 98.0N 28.0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH1) (TDOH2) (TDOH3) (TPOH) (TRC) (TWC)	132.N 130.N 132.N 130.N 224.N 200.N	102'N 100'N 114'N 108'N 200'N	28,0% 28,0% 30,0% 32.0% 120.0 120.0
IIL	IIH	VIC1	AICS	
ANQ_E8= SA ANQ_18= SA	79.4NA 77,1NA 77,5NA 83.9NA	2.47 V 2.50 V 2.52 V 2.50 V	52,46 V 52,52 V 52,56 V 52,55 V	
A5 #84,9NA A6 #82,0NA	91.9NA 77,7NA 75,5NA 79.8NA	2.50 V 2.44 V 2.47 V 2.46 V	#2,51 V #2,49 V #2,51 V #2,51 V	
CS2 =81.0NA MWR =81.7NA	81,5NA 82,9NA 73,7NA 76,8NA	2.48 V 2.51 V 2.45 V 2.46 V	=2,49 V =2,52 V =2,48 V =2,48 V	
DI1 #78,3NA DI2 #77,8NA	79.5NA 77.3NA 74.9NA 74.3NA	2.57 V 2.54 V 2.57 V 2.54 V	#2,52 V #2,53 V #2,53 V	

RÇA	CDP1822SD	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP:	125 C S
					PAGE	10 OF 10
	000	001	500	200		
AOH5 AOH1 AOF5 AOF1	115.MV 125.MV 4.82 V 9.73 V	120 MV 140 MV 4,82 V 9,73 V	130.MV 165.MV 4.82 V 9.72 V	130,MV 155.MV 4,82 V 9,74 V		
10N2 10P1 10P2	6.45MA 14.9MA -2.23MA -4.74MA	6,15MA 13,6MA -2,23MA -4,74MA	5.65MA 11.7MA =2.16MA =4.53MA	5.80MA 12.2MA =2,22MA =4.77MA		
1021 1022 1023 1024	1.94UA 1.91UA 1.92UA 1.90UA	2,13UA 2,14UA 2,13UA 2,14UA	AUQ5.5 AU15.5 AU15.5 AUQ5.5	2,12UA 2,13UA 2,13UA 2,13UA		
1025 1026 1027 1028	1,97UA 1,99UA 1,96UA 1,95UA	2,20UA 2,21UA 2,19UA 2,19UA	2.31UA 2.28UA 2.26UA 2.25UA	2,25UA 2,19UA 2,19UA 2.19UA		
ILDP	40.0UA					
IL1 IL2 IL3 IL4	≈90.0UA ≈120.UA ≈150.UA ~135.UA					

5N:

RCA	CDP1822SD	256 X 4	CMOS	STATIC RAM	31	AUG 78	TEMPi	25 C.	SNI	15

RÇA	CDP1822SD	256 X 4	CMOS	STA	FIC RAM	31	AUG 78	TEMPi	25 C	
								PAGE	1 OF	10
		(WIDE LI	MITS	VC	C=10V			UIII Yearn	AN THE	
	D GALPAT	(TIGHT LI			=10V		REFRED	ucerlity L Page I	T TITES	
PAGGE	D GALPAT	(TIGHT LI	MITSI	VC	2=5V		報びび連続	Trucks =	2004	
PASSE	DATA RET	ENTION TE	ST					,		
				vcc	= 4 ₄ 5V		5', Ø	v	iøʻ.øv	l
ADDRE	SS ACCESS	TIME	(TAA)		195.1	V	160	N	70:01	•
	SETUP TIME		(TDS)		20,01		16.		8.00N	
DATA	HOLD TIME		(HQT)		8,001	J	8.0		10.0N	
ADDRES	SS SETUP T	IME	(TAS1)	18,0	J	12.	ØIN:	4.90	l
	SS SETUP T		(TASE		96,01	ļ	82.		40.0N	
	SS MOLD TI		(TAH)		96,01 +14,01	1	m10.		-2.00N	
WRITE	PULSE WIN	ተዛ -	(TWP)		62,04	J	54.	ØN	34,0N	
CS1	SETUP TIM	E	(TCSS	1)	432.1	J	354	, N	72,0N	
CS2	SETUP TIM	E	(TESS		210.1		164		60,0N	
	HOLD TIME		(TCSH	1)	40,0N	1	36.		24,0N	
CSS i	HOLD TIME		(TCSH	5)	40.01		36.	ŅΝ	25. ต _ั ท	
OUTPU	ACTIVE F	ROM CS1	CTDOA	1)	176.N	J	152	' N	82,0N	
	F ACTIVE F		(TDOA		172.1		150	- N	82,0N	
ՕԱ †ԲԱ1	ACTIVE F	ROM MRD	(TDDA	3)	38.01	1	34.1		25.00	
OUTPU	Г НОЦО РВО	M CS4	(TOOH	in	122.1	1	92.	21 N.!	20,0N	
	HOLD FROM		(TOOH		150.1		95.		22, ØN	
	HOLD FROM		(TDOH	-	130 N		110	_ N	28,0N	
	HOLD FROM		(TPDH		126.N		196	- N	28,ØN	
READ (CYCLE TIME		(TRC)		200 N		176	N	112.N	
WRITE	CYCLE TIM	E	(TWC)		184.N		176	N	104.N	
	714	IIH			VICI		VICP			
ΑØ	≈2,00NA	1,5	DNA .		2.77 V		-2,78	ı		
A1	-1.BUNA	1,8			2.80 V		#2,83 \			
4 5	4 5 5 5 1 1 1	777								

	714	IIH	VICi	VICP
A0	ANDO.50	1,50NA	2.77 V	+2,78 V
A1	ANDB.10	1,80NA	2.80 V	+2,83 V
A2	ANDB.10	1,60NA	2.82 V	+2,86 V
A3	ANDO.50	2,10NA	2.85 V	+2,87 V
A4	-2.20NA	1 70na	2.82 V	#2,84 V
A5	AND9.1=	1,90na	2.73 V	#2,83 V
A6	AND7.1=	2,20na	2.73 V	#2,76 V
A7	AND7.1=	2,20na	2.75 V	#2,77 V
CS1	=1,60NA	1.90NA	2,76 V	-2,77 V
CS2	=2,00NA	1.80NA	4.96 V	-4,95 V
MWR	=1,70NA	1.60NA	2.78 V	-2,80 V
MRD	=1,70NA	1.60NA	2.77 V	-2,78 V
DIØ	=1.80NA	1.70NA	2,84 V	#2,80 V
DI1	=1.70NA	1.80NA	2,83 V	#2,79 V
DI2	=1.90NA	1.60NA	2,81 V	#2,80 V
DI3	=1.90NA	1.80NA	2,82 V	#2,77 V

RCA	CDP18228D	256 X 4	CMOS	STATIC	RAM 3	1 AUG	78	TEMP:	25 C	SNI	15
								PAGE	2 05	10	
	กิตฮ	001		מחי	,	D	03				

	បិព្គ៧	001	פֿטט	D03
VOL 1	75.0MV	80,0MV	85.0MV	85.PMV
VOLA	85.0MV	95,0MV	110.MV	105.MV
VOHI	4.88 V	4.88 V	4.88 V	4,88 V
SHOV	9.81 V	9.82 V	9.91 V	9 82 V
IDN1	9,65MA	9',35MA	8_55MA	8'.70MA
IDMS	21.7MA	20.1MA	17.3MA	18 0MA
IDP1	=3.11MA	-3,18MA	-3.05MA	-3,21MA
Squi	#6.65M∧	-6.82MA	76.48MA	-6.91MA
IOZi	51.7NA	63,9NA	53,7NA	62,2NA
IOZZ	53,7NA	60,9NA	55,6NA	60.1NA
1073	54.7NA	58 3NA	59,0NA	56.0NA
1024	51.4NA	62,0NA	55.2NA	59.6NA
1075	56,9NA	58.7NA	59, 8NA	60, INA
1026	57 4NA	58.9NA	59,7NA	58.5NA
IUZ7	57.7NA	58.4NA	59,4NA	58.3NA
1028	56 4NA	58.2NA	59.4NA	57.9NA

ILDP ⊨5.00UA

IL1 =5.00UA IL2 =5.00UA IL3 =5.00UA IL4 =5.00UA

PAGE 3 OF 10

PASSED	GALPAT	CWIDE	LIMITS)	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS)	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS	VCC=5V

A MANOR DATA NETER	1104 1201			
	vc	C = 4,5V	5'.ØV	10'.0V
ADDRESS ACCESS TIN	(TDS)	185.N 20.0N	150'.N 16.0N	65.0N
DATA HOLD TIME	(HOH)	6,00N	8.09N	10.0N
ADDRESS SETUP TIME	· ·	16.0N	12.0N	4.00N
ADDRESS SETUP TIME ADDRESS HOLD TIME	E (TAS2) (Tah)	90,0N +12,0N	74.0N =10.0N	M0.8€ M00.5÷
WRITE PULSE WINTH	(TWP)	65.0N	54.0N	32.0N
CS1 SETUP TIME	(TCSS1)	134.N	114'N	58, ØN
CS2 SETUP TIME	(TCSS2)	132.N	112.N	54,0N
CS1 HOLD TIME	(TCSH1)	38,ØN	34,0N	22,0N
CS2 HOLD TIME	(TCSH2)	38.ØN	34.9N	22.0N
OUTPUT ACTIVE PRO	4 CS1 (TDOA1)	170 a N	146.N	40,0N
OUTPUT ACTIVE FROM	=	168.N	142.N	78, ØN
OUTPUT ACTIVE FROM	MRD (TDDA3)	34.ØN	32.0N	20.0N
OUTPUT HOLD FROM (S1 (TDOH1)	116 N	86.0N	20,0N
OUTPUT HOLD FROM (86. ØN	20,0N
OUTPUT HOLD FROM N		••	108 N	26,0N
OUTPUT HOLD FROM N READ CYCLE TIME	1WR (TPDH) (TRC)	124.N 192.N	194,N	28.0N
WRITE CYCLE TIME	(TWC)	176 N	168.N 168.N	104.N 96.0N
7 > 1	V #1;	UTDA		
7.1.L	ITH	VIC1	VICE	
A0 -400 PA	200,PA	2.84 V	#2,85 V	
A1 4300.PA	300,PA	2.88 V	+2,89 V	
A2 =300.PA A3 =400.PA	200,PA 300.PA	2.89 V 2.91 V	-2,92 V -2,93 V	
אומטשריי שה	JODET H	E # 74 Y	- C 6 3 7 V	
A4 -600.PA	200 PA	2.89 V	#2,89 V	
A5 =400.PA	300.PA	2.80 V	•2,89 V	
A6	400 ₂ PA 400 . PA	2.80 V 2.83 V	-2,83 V -2,84 V	
CS1 ~200.PA CS2 ~300.PA	300 PA	2.84 V	-2,84 V	
CS2 =300.PA MWR =300.PA	300.PA 200.PA	2.86 V 2.85 V	=2.89 V	
AQ, DOE- DAM	300.PA	2.85 V	⊕2,87 V =2.85 V	
DIO 9300,PA	200 PA	2 <u>.</u> 91 V	-2,87 v	
DI1 -300.PA	300 PA	2.89 V	#2,86 V	
012 -300.PA	200 PA	2.89 V	-5'86 A	
DI3 -300 PA	300.PA	2.89 V	-2.84 V	

RCA	CDP1822SD	256 X 4 CMOS	STATIC RAM 3	11 AUG 78	TEMP	-20 C	SN:	15
					PAGE	4 OF	10	- -
	DOM	001	poa	003				:
VOL 1	65.0MV 75.0MV	70.0MV 80.0MV	75,0MV 95,0MV	75.4MV 90.4MV				: •

		4 CO # CO 11 A	ייטאַניי	1 7 8 811 A
VOLE	75.0MV	80.0MV	95.ØMV	9g ู ดหง
VUHI	4.89 V	4.90 V	4.89 V	4,90 V
VUH2	9.84 V	9.85 V	9.84 V	9.85 V
A 1511E	7.404 7	4 * O T A	7 . OM Y	י רים∗ל
IDNI	11,1MA	10.7MA	9.85MA	10.0MA
IDNS	25.2MA	23.3MA	AMS.0S	20.9MA
IDPI	-3.68MA	-3,76MA	#3.69MA	-3,81MA
	-	•		
IDP2	∝7.83MA	-8.04MA	-7.69MA	#8.15MA
1021	7.40NA	7.00NA	7.80NA	5.20NA
-	·	•	•	
1025	4 . 1 @ N A	:0.3NA	4,40NA	8,40NA
1023	9.80NA	5.30NA	5.10NA	5,5004
1074	9 90NA	3.90NA	10.0NA	3.70NA
1025	3.30NA	1.0.9NA	3,50NA	11.3NA
			•	
1026	3,60NA	11.2NA	3.20NA	10.8NA
1077	3.30NA	11.1NA	3.40NA	11,1NA
IOZB	3.50NA	11.2NA	3.iONA	10.7NA
- · -	- -		TO BE A SHIP TO	- 1. R . 1. W

ILDP	-15.0UA
T (** 17.1	~ といるのけい

ILi	⇒5.00UA
ILS	₩5,00UA
IL3	-5.00UA
IL4	+5.00HA

PAGE 5 OF 10

PASSED	GALPAT	(WIDE	LIMITS)	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS)	ACC=10A
PASSED	GALPAT	(TIGHT	LIMITS)	VCC=5V

ORIGINAL PAGE IS POOR

	vcc	* 4.5V	5'.0V	10'.0V
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(AAT) (TDS) (HDT)	175.N 24'.0N 6.00N	145'.N 18.0N 6.00N	60.0N 6.00N 10.0N
ADDRESS SETUP TIME ADDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WIDTH	(TAS1) (SAST) (HAT) (HHT)	14,0N 86,0N -12,0N 54.0N	10.0N 70.0N -10.0N 56.0N	4 . 00 N 32 . 0 N 32 . 0 N 30 . 0 N
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS1) (TCSS2) (TCSH1) (TCSH2)	128.N 126.N 42.0N 42.0N	108, N 106. N 34. ON 34. ON	54,0N 52,0N 22,0N 20,0N
OUTPUT ACTIVE FROM CSE OUTPUT ACTIVE FROM MRC	(SAOOT)	166.N 162.N 32.ØN	136,N 134.N 30,0N	76,0N 74,0N 20,0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRO OUTPUT HOLD FROM MWR OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH1) (TDOH2) (TDOH3) (TPOH) (TRC) (TWC)	110.N 108.N 128.N 124.N 184.N	82.0N 82.0N 108.N 104.N 144.N 168.N	18.0N 26.0N 26.0N 26.0N
IIL:	IIH	VICI	AICS	'
A1 =100.PA :	100,PA 100,PA 100,PA 100.PA	2.91 V 2.94 V 2.95 V 2.97 V	22,95 V 22,95 V 22,98 V	
AS #100.PA :	100.PA 100.PA 100.PA 100.PA	2.95 V 2.88 V 2.87 V 2.89 V	#2,95 V #2,95 V #2,90 V #2,91 V	
CS2 ≈100.PA : MWR ≈100.PA :	100 PA 100 PA 0 00 A 100 PA	2.90 V 2.93 V 2.91 V 2.91 V	#2,95 V #2,95 V #2,93 V	
DI1 0.00 A 1	100, PA 100, PA 100, PA 100, PA	2.98 V 2.96 V 2.95 V 2.95 V	2,93 V 2,93 V 2,93 V 2,91 V	

RCA	CDP1822SD	256 X 4 C	MOS STATIC	RAM 31 AÚC	78 TEMPI
					PAGE
	េ្ធព្រ	001	sad	t	2003
VOL1 VOL2 VOH1	60',0MV 65',0MV 4.91 V 9.87 V	60.0M 70.0M 4,91 9.87	V 85° 1 V 4.9	9MV 8	55.0MV 30.0MV 1.91 V 3.88 V
IDN1 SNOI IDP1 SPOI	12,3MA 28,3MA =4,23MA =8,97MA	12,0M 26,3M +4,39M -9.24M	A 11,1 A 22,1 A #4.2	2MA 18 6 AMA 26 74 AM6	1.2MA 23.7MA 1.44MA
IOZ1 IOZ2 IOZ3 IOZ4	6.60NA 3.70NA 900.PA 4.50NA	-800,P 600,P 4,30N 600,P	A 4.11 A -700	ØNA ⇔6 •PA 4	300, PA 300, PA 4,50NA 1,20NA
1025 1026 1027 1028	10.2UA -700.PA -800.PA -500.PA	10.2U 5.80N 5.40N 5.30N	A -1.50	ZNA 9	0 204 5 80NA 5 90NA 5 50NA
ILOP	-10.0UA				

-5,00UA -5,00UA -5,00UA

IL1 IL2 IL3 IL4 15

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SNI

6 OF 10

PASSED	GALPAT	(WIDE	LIMITS)	VCC≈1ØV
PASSED	GALPAT	(TIGHT	LIMITS	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS)	VCC≈5V

	VCC	= 4.5V	5.0V	10'.0V
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA) (TDS) (TDH)	185.N 20.0N 10.0N	160.N 18.ON 10.ON	0.08 0.08 12.08
ADDRESS SETUP TIME ADDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WIDTH	(TAS1) (TAS2) (TAH) (TWP)	10'.0N 98,0N -14.0N 70.0N	8'.00N 88.0N +12.0N 62.0N	4.00N 46.0N -2.00N 38.0N
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS1) (TCSS2) (TCSH1) (TCSH2)	140 N 138 N 48 ON 50 ON	124, N 122. N 44. MN 46. MN	68, 0N 66, 0N 30, 0N 28, 0N
OUTPUT ACTIVE FROM CS1 OUTPUT ACTIVE FROM CS2 OUTPUT ACTIVE FROM MRO	(SACOT)	184 "N 180 "N 42 " ON	164° N 160° N 38° ON	90,5N 88,0N 26,0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH1) (TDOH2) (TDOH3) (TPOH) (TRC) (TWC)	124	94.0N 94.0N 112,N 106,N 184,N 176.N	1.00K 30.0N 30.0N 22.0N
IIL	ITH	VICI	VICE	
A1 -22,3NA 2 A2 -22,5NA 2	20.8NA 22.5NA 22.6NA 23.4NA	2.73 V 2.77 V 2.79 V 2.81 V	92,74 V 92,79 V 92,83 V 92,84 V	
A5 -22,7NA 8 A6 -21,9NA 8	21.9NA 22.7NA 22.3NA 22.9NA	2.79 V 2.69 V 2.69 V 2.72 V	=2.80 V =2.78 V =2.73 V	
CS2 =21,1NA 2 MWR =21,3NA 2	21.8NA 22.6NA 21,8NA 20.3NA	2,73 V 2,75 V 2,74 V 2,74 V	-2,74 V -2,80 V -2,77 V -2.74 V	
AN2,05- 110 AN0,15- SIQ	21.0NA 21.7NA 20.2NA 21.3NA	2.80 V 2.79 V 2.78 V 2.78 V	-2,76 V -2,76 V -2,76 V -2,74 V	

RCA	CDP1822SD	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP	85 C 8N:
					PAGF	8 OF 10
	000	001	son	003		
VOL 1	90.0MV	95.0MV	105.MV	100'MV		
AOF 5	105.MV	110.MV	130 MV	125.MV		
VOH1	4.85 V	4 86 V	4.85 V	4,86 V		
AOHŞ	9.78 V	9.78 V	9.77 V	9.78 V		
IDN1	8.2044	7.90MA	7.20MA	7'.35MA		
IDNS	18.3MA	16.9MA	14.5MA	15.184	•	
TUP1	~	-2,65MA	₩2.59MA	≈2,69MA		
IDES	⇔5.58MA	-5.73MA	#5.47MA	-5.82MA		
1071		649, NA	644.NA	654°NA		
Inza	609.NA	642.NA	640.NA	638,NA		
1023	606 NA	646.NA	644.NA	636.NA		
1024	608.NA	647 NA	639.NA	644.NA		
1025		655, NA	662.NA	665, NA		
1026	616.NA	670 NA	649.NA	655,NA		
IUZ7	609 NA	658,NA	654.NA	645 NA		
1028	618.NA	657.NA	649.NA	653.NA		
91 BB	20.004					
ILOP	50.0UV					
IL1	-25.0UA					
175	=30,0UA					
IL3	-30.0UA					
IL4	-25.0UA					

RCA	CDP18228D	256	X	4	CMOS	STATEC	RAM	31	AUG	78	TEMP:	125	£	SNI	15
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PAGE 9 0F 10

PASSED GALP PASSED GALP PASSED GALP	AT (TIGHT AT (TIGHT	LIMITS) LIMITS)	VCC=10V VCC=10V VCC#5V	REPRODUCIBILITY ORIGINAL PAGE 1	
PASSED DATA	RETENTION	TEST			
		V	CC = 4.5V	5.0V	10'.0V
DATA SETUP DATA HOLD T	TIME	(TAA) (TDS)	195.N 22,0N	175 N 18.0N	90,00 8.00N
17 M 1 M 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	∔ "15	(TDH)	12.0N	12.0N	14.0N
ADDRESS SETT ADDRESS SETT ADDRESS HOLD WRITE PULSE	UP TIME D TIME	(TAS1) (SCAT) (HAT) (GWT)	8.00N 104.N =16.0N 74.0N	8'.000 .96.00 ~14.00 68.00	4.00N 50.0N -4.00N 42.0N
	TIME TIME TIME TIME	(TCSS1) (TCSS2) (TCSH1) (TCSH2) 144.N) 52.0N	132°, N 128°, N 46°, AN 48°, AN	74,0N 70,0N 30,0N 30.0N
OUTPUT ACTION OUTPUT ACTION ACTION	VE FROM CS2	SADOTE	194 ใ	178, N 174. N 42. ØN	100.N 96.0N 26.0N
OUTPUT HOLD OUTPUT HOLD OUTPUT HOLD OUTPUT HOLD READ CYCLE T	FROM CS2 FROM MRD FROM MWR ITME	(TDOH1) (TDOH2) (TDOH3) (TPDH) (TRC) (TWC)	N.857 (98.0N 98.0N 114.N 108.N 192.N 184.N	24,0N 24,0N 30,0N 32,0N 120.N
11L	I	TH	VICI	vtcz	
AØ -127, A1 -127, A2 -129, A3 -128,	NA 1	18.NA 21.NA 23.NA 24.NA	2.72 V 2.76 V 2.77 V 2.80 V	-2,72 V -2,78 V -2,81 V -2,83 V	
A4 -125, A5 -126, A6 -125, A7 -120,	NA 1	18.NA 21,NA 19,NA 18.NA	2.78 V 2.67 V 2.67 V 2.70 V	=2,79 V =2,77 V =2,70 V =2,71 V	
CS1 -129. CS2 -122. MWR -122. MRD -122.	NA 1	18, NA 22, NA 18, NA 14. NA	2.71 V 2.73 V 2.73 V 2.72 V	-2,72 V -2,78 V -2,76 V -2.73 V	

2.79 V 2.77 V 2.76 V 2.77 V

=2,74 V =2,74 V =2,74 V =2,72 V

*118.NA -118.NA -116.NA +116.NA 117.NA 117.NA 110.NA 113.NA

REA	CDP1822SD	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP	125 C	SN
					PAGE	10 OF	i Ø
	DOØ	001	500	003			
VOL1 VOL2 VOH1 VOH2	100.MV 115.MV 4.82 V 9.75 V	105.MV 125.MV 4.84 V 9.76 V	115.MV 150.MV 4.83 V 9.74 V	115, MV 145, MV 4,84 V 9,76 V			
IDN1 IDN2 IDP1 IDP2	7.25MA 16.2MA -2.31MA -5.03MA	7.00MA 14.9MA -2.39MA -5.16MA	6.40MA 12.8MA -2.31MA -4.89MA	6.50MA 13.4MA 42.40MA -5.22MA			
10Z1 10Z2 10Z3 10Z4	2,61UA 2,59UA 2,59UA 2,59UA	2.76UA 2.77UA 2.75UA 2.76UA	2.73UA 2,72UA 2.73UA 2.73UA	2,71UA 2,71UA 2,71UA 2.72UA			
1025 1026 1027 1028	2.64UA 2.66UA 2.63UA 2.62UA	2,80UA 2,82UA AUN8,5	2.81UA 2.78UA 2.77UA 2.76UA	2,81UA 2,76UA 2,76UA 2,76UA			
ILDP	40.0UA						
IL1 IL2 IL3 IL4	=105.UA =115.UA =125.UA =100.UA						

					•
RCA C	DP18228D 256	X 4 CMOS STA	TIC RAM	31 AUG 78 TEMPI	25 C SN:
		1		PAGF	1 OF 10
PASSED		T LIMITS) VO	C=10V C=10V		
PASSED	GALPAT (TIGH	T LIM its) VC	C≈5V		
PASSED	DATA RETENTIO	N TEST	9.		
		VCC	= 4.5V	5.0v	10.0V
	S ACCESS TIME ETUP TIME	(TAA) (TDS)	295.N 36./ // N	240' ₋ N 28.0N	95,0N 10,0N
	OLD TIME	(TDH)	36,0N 10.0N	10.0N	10.0N
	S SETUP TIME S SETUP TIME	(TAS1)	18.0N 138.N	14,9N 112,N	4.00N 52.0N
AUDRES	S HOLD TIME	(TAH)	-26,0N	-Pa.an	⇔6.00N
WRITE	PULSE WINTH	(TWP)	96.0N	87.AN	42,0N
	ETUP TIME ETUP TIME	(TCSS1) (TCSS2)	218 ₈ N	178, N	80.0N
	OLD TIME	(TCSH1)	254.N 62.ØN	214.N 54.0N	107.N 38.0N
CS2 H	OLD TIME	(TCSH2)	0.00	o ๋ ถด	0.00
QUTPUT			278 N	232,N	104.N
	ACTIVE FROM C ACTIVE FROM M	-	314.N 62.0N	266.N 54.0N	122.N 30.0N
	HOLD FROM CS1	(TDOH1)	166 _n N	132 N	40,0N
	HOLD FROM CS2 HOLD FROM MRD	(SHOOT) (SHOOT)	232.N 142.N	204,N	92,0N
OUTPUT	HOLD FROM MWR	(TPOH)	142 N	122,N 118,N	34,0N 36.0N
	YCLE TIME CYCLE TIME	(TRC)	312 N	ا4م256	128.N
MATIC		(TWC)	304.N	280 <u>'</u> N	120.N
	IIL	IIH	AICI	VICS.	
AØ A1	-3.00NA -2.80NA	2.60NA 3.00NA	3.40 V 3.44 V	=3,40 V =3,44 V	
Ã2	=2.60NA	2,80NA	3,48 V	ლ3°,44 V ლ3°,49 V	
A3	#2,8ØNA	2.70NA	3.47 V	-3.48 V	
A4 A5	-2,70NA	2.70NA	3.44 V	-3,47 V	
A 6	#3,00NA =2,70NA	2,60NA 2,30NA	3.37 V 3.43 V	93,41 V 93,34 V	
A 7	-2.90NA	2.70NA	3.41 V	=3 43 V	
CS1 CS2	+2.50NA	2.90NA	3.47 V	=3,45 V	
MWR	⇒2.80NA ⇒2.80NA	4,50NA 2,60NA	4,96 V 3,41 V	44,95 V 43 V	
MRD	-2,50NA	2,50NA	3.42 V	#3.42 V	
010	-2,80NA	2,60NA	3.54 V	-3,48 V -3,48 V	
DII	#3.00NA #2.70NA	2,40NA 2,80NA	3,53 V 3,49 V	⊕3°μ48 V ⊕3°μ46 V	
013	#3,30NA	2.40NA	3.45 V	#3.44 V	
			D 161		

RCA	CDP1822SD	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP	25 C SN:	16
					PAGF	2 OF 10	
	non	001	200	003			
VQL1	115.MV	115.MV	125.MV	120, MV			
AOL 5	115.MV	125 MV	140.MV	135.MV			
VOHI	4.82 V	4,82 V	4.82 V	4 82 V			
AOHS	9,76 V	9.76 V	9.76 V	4'82 V 9'77 V			
IDNI	6.50MA	6.35MA	6.00ма	6.10MA			
IDNE	16.2MA	15.2MA	13.8MA	14,1MA			
TUP 1	WIS BE	-2.23MA	-2.18MA	-2.24MA			
IDP2	₩5.22MA	-5.27MA	45.13MA	-5.33MA			
IUZ1	21.7NA	28,9NA	20,5NA	26,9NA			
IOZZ	23,9NA	26,1NA	22.5NA	24,3NA			
1023	25,1NA	23.8NA	22,5NA 25,2NA	20.3NA	,		
1024	55°0NY	27.4NA	21.6NA	23.7NA			

24,4NA 24,7NA 24,1NA 24.5NA

ANP.55 ANP.55 ANP.55 ANP.55

23.5NA 23.7NA 23.6NA 23.7NA

ILDP -2,00UA

ANE, 65 ANS, 65 ANO, 65 ANO, 65

1075

10Z6 10Z7 10Z8

IL1 IL3 -5,00UA -5.00UA ~5.00UA ~5.00UA IL4

PAGE 3 OF 10

PASSED GALPAT (TIGH	T LIMITS) VO T LIMITS) VO	C=10V C=10V C=5V	reproducibil Original pag	
PASSED DATA RETENTIO			•	
	VÇC	: = 4.5V	5.ØV	10.0V
ADDRESS ACCESS TIME	(TAA)	320.N	245[N	85.0N
DATA SETUP TIME	(TDS)	42, ØN	32.0N	400.8
DATA HOLD TIME	(трн)	8 * 00 N	8.00N	10.0N
ADDRESS SETUP TIME	(TAS1)	32.0N	5น์ " นัก	4.90N
ADDRESS SETUP TIME	(TAS2)	146 N	114.N	48,0N
ADDRESS HOLD TIME	(TAH)	-26.0N	₩20 mN	=4.00N
WRITE PULSE WINTH	(TWP)	106.N	84,00	38,0N
CS1 SETUP TIME	(TCSSi)	218 N	172, N	74, ØN
CSS SETUP TIME	(TCSS2)	266.N	N.585	105.N
CS1 HOLD TIME	(TCSH1)	54.0N	46.0N	26.0N
CS2 HOLD TIME	(TCSH?)	ଉ ଅପ	ଡ୍ଲୁଡ଼େଉ	0.00
OUTPUT ACTIVE FROM C	S1 (TDOA1)	284.N	888 [°] N	96.0N
OUTPUT ACTIVE FROM C	S2 (TOOAZ)	340.N	274 N	114.N
OUTPUT ACTIVE FROM N	RD (TDDA3)	58.ØN	50.AN	56, QN
OUTPUT HOLD FROM CSt	(100H1)	158.N	124'N	38,0N
OUTPUT HOLD FROM CS2		248.N	124,N 212,N	104.N
OUTPUT HOLD FROM MRD		142.N	120 _± N	34,0N
OUTPUT HOLD FROM MWR	• • • • •	138,N	N م 116 N	32.0N
READ CYCLE TIME	(TRC)	296 N	240,N	120.1
WRITE CYCLE TIME	(TWC)	304.N	248.N	112.N
TIL	IIH	vici	VICZ	
AØ -400.PA	300.PA	3.42 V	-3,41 V	
A1 -300.PA	300,PA	3.46 V	-3,45 V	
A2 -300.PA	300.PA	3.49 V	93,50 V	
A3 +300.PA	300 PA	3_48 V	-3.49 V	
A4 =300.PA	500,PA	3.46 V	48 V	
A5 ~300.PA	300.PA	3.38 V	-3,43 V	
A6 +300,PA	200,PA	3,44 V	۷ 88وچ	
A7 =500.PA	300.PA	3_42 V	=3,44 V	
CS1 -300.PA	300 PA	3.48 V	45 V م	
CS2 -400.PA	1.00NA	4.96 V	+4,95 V	
MWR -300.PA	300,PA	3.42 V	#3,44 V	
MRD #300.PA	300.PA	3.44 V	₩3.43 V	
DIM =3MM.PA	300,PA	3.55 V	-3,48 V	
DI1 =500.PA	200 PA	3.54 V	#3,48 V	
DI2 =300.PA	400,PA	3.50 V	-3,46 V	
DI3 +400 PA	200.PA	3.46 V	-3.44 V	
		B-153		

RCA	COP1822SD	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP	⇒èø c	SNI	16
					PAGE	4 OF	10	
	Dog	100	noe	003				
VOL 1	100.MV	105.MV	110.MV	105,MV				
VOLS	100.MV	110.MV	120 MV					
VOHI	4.85 V	4.86 V	4.85 V	4.85 V				
SHOV	9.80 V	9'.80 V	9,80 V	115.MV 4.85 V 9.80 V				
IDN1	7.20MA	7.05MA	6.75MA	6.80MA				
IDNS	18.4MA	17,4MA	15.8MA	16.3MA				
70P1	48.61MA	-2,63MA	92.61MA	-2,64MA				
1072	≈6.19MA	-6,25MA	-6.13MA	-6.31MA				

5.8ØNA 8.10NA 800.PA

2.00NA

3.20NA 700.PA 7.70NA 6.10NA

1,20NA 1,10NA 1,10NA 900.PA

1025 1026 1027 1028	6.30NA 6.20NA 6.30NA 6.20NA	2,30NA 2,80NA 2,20NA 2,30NA	6.60NA 6.70NA 6.60NA 6.80NA
ILDP	~5.00UA		
ILI IL3	-5,00UA -5,00UA -5,00UA		

3,20NA 1,30NA 8,60NA 6,10NA

7.10NA 7.70NA 1.20NA

3.50NA

-5,00UA

TOZ1 TOZ2 TOZ3

IUZ4

ILA

PAGE 5 OF 10

PASSED	GALPAT	(WIDE	LIMITS)	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS)	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS)	VCC=5V

A HEARD CHINA CHINESTS	U			
	VC	: = 4.5V	5.0v	10.0V
ADDRESS ACCESS TIME	(TAA)	325.N	240'N	80,0N
DATA SETUP TIME	(TDS)	56. ØN	3A. ØN	8,001
DATA HOLD TIME	(HOH)	6 00N	6 09N	8.00N
SATE OF THE	(1.311)	បូត្ខ សម្នាក	da 🖩 de serie	0 8 20 14
ADDRESS SETUP TIME	(TAS1)	36.0N	18. AN	4.ØØN
ADDRESS SETUP TIME	(SEAT)	142.N	. 108 N	42.0N
ADDRESS HOLD TIME	(TAH)	⇔26.ØN	#50 * UP	=4.00N
WRITE PULSE WINTH	(TWP)	120.N	76. MN	38,0N
PC4 PETIM TRUE	emment	202 1	4.6 11.5	3a' au
CS1 SETUP TIME	(TESSI)	220 N	164,N	70,0N
CSS SETUP TIME	(TCSS2)	284.N	535.N	10P.N
CS1 HOLD TIME	(TCSH1)	54.0N	5 2. 0N	24.0N
CS2 HOLD TIME	(TCSH2)	0.00	ଉ.ଡନ	0.00
OUTPUT ACTIVE FROM	CS1 (TDOA1)	288 N	a≥a, N	88.0N
OUTPUT ACTIVE FROM		342.N	270.N	
OUTPUT ACTIVE FROM	_	•	·	112.N
DOTECT ALTIVE PROM	MRD (TOOA3)	54. ØN	46.3N	24.0N
OUTPUT HOLD FROM CS	(TDOH1)	152.N	118,N	34.0N
OUTPUT HOLD FROM CS	(SHOOT)	262.N	224, N	112.N
OUTPUT HOLD FROM NR		140 N	118,N	30,0N
OUTPUT HOLD FROM MW	•	138.N	114 N	32.ØN
READ CYCLE TIME	(TRC)	280.N		120.N
WRITE CYCLE TIME	(TWC)	350°N	224,N 280.N	•
MEXIC CICE 1100	(1WL)	250 ° 14	ዲ ሁ A: * IA	104.N
IIL	IIH	VIC1	VICA	
AØ =100.PA	100.PA	3.46 V	-3,45 V	
A1 -100.PA	100.PA	3.50 V	=3,49 V	•
AZ Ø.ØÔ A	100 PA	3.53 V	-3,54 V	
A3 =100,PA	100.PA	3.52 v	-3.52 V	
			•	
A4 mind.PA	100,PA	3.50 V	-3,51 V	
A5 -100.PA	100.PA	3.42 V	≈3°47 V	
A6 =100.PA	100 _e PA	3.47 V	≈3°,43 V	
A7 =100.PA	100.PA	3.46 V	-3,48 V	
CS1 =100.PA	100,PA	3.52 V	-3 45 V	
CS2 #100.PA		•	=3.49 V	
	400,PA	4.97 V	=4,95 V	
	100,PA	3.46 V	#3,48 V	
MRD →100.PA	100.PA	3.48 V	-3.47 V	
DIO -100.PA	100.PA	3.58 V	-3,51 V	
DI1 -100.PA	100 PA	3.57 V	-3,51 V	
DIS 0.00 A	100,PA	3,54 V	=3,49 V	
DI3 -100.PA	100 PA	3 50 V	-3.48 V	
4 W E G 1 74	a wase man	34 314 4	Mr. B. Adric. A.	

RCA	CDP1822SD	256 × 4	CMOS	STATIC	RAM 31	AUG	78	TEMP:	-55 0	SN:	16
								D 4 0 0	4 65	4.61	

	poa	001	DOS	003
AOF 3	95.0MV	95.0MV	100.MV	100 MV
	95.0MV	100.MV	105.MV	105 MV
	4.87 V	4.88 V	4.87 V	4,88 V
	9.84 V	9.84 V	9.82 V	9.84 V
ION1	7.80MA	7,65MA	7.35MA	7'.45MA
IDN2	20.3MA	19.3MA	17.7MA	18.1MA
IDP1	=3.01MA	-3,05MA	-3.03MA	-3,06MA
IDP2	=7.15MA	-7,25MA	-7.13MA	-7.32MA
1071	6.20N4	-500,PA	4.90NA	-400 PA
1072	4.40NA	-800.PA	4.90NA	-1,70NA
1073	-600.PA	5.00NA	-1.60NA	4,90NA
1074	2.80NA	1.80NA	1.20NA	2,20NA
1025	2.00NA	1.30NA	2.50NA	300 PA
1026	1.90NA	1.60NA	2.60NA	*100 PA
1027	2.00NA	1.20NA	2.50NA	200 PA
1028	1.90NA	1.40NA	2.60NA	*100 PA
ILDP	-10.0UA			
IL1 IL2 IL3 IL4	=5.00UA ⇒5.00UA =5.00UA ≈5.00UA			

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PAGE 7 OF 10

PASSED GALPAT (TIGH	IT LIMITS) VC IT LIMITS) VC	C=10V C=10V C=5V	REPRODUCIBIL ORIGINAL PAG	ITY OF THE E IS POOR
PASSED DATA RETENTIO	IN TEST			
	ACC	= 4,50	5. pv	10,0V
ADDRESS ACCESS TIME	(AAT)	280 N	235°N	105.N
DATA SETUP TIME	(TDS)	38,0N	30,0N	10,0N
DATA HOLD TIME	(HQT)	12.0N	12.0N	12', ØN
ADDRESS SETUP TIME	(TAS1)	10 . ON	8. MAN	4 . ØØN
ADDRESS SETUP TIME	(TAS2)	149 . N	120 N	60.0N
ADDRESS HOLD TIME	(YAH)	-26.0N	-20.9N	-6.00N
WRITE PULSE WIDTH	(TWP)	104 N	92.an	48, ØN
CS1 SETUP TIME	(TCSS1)	1.00K	184°N	88, 00
CS2 SETUP TIME	(TCSS2)	214.N	180.N	86, ØN
CS1 HOLD TIME	(TCSH1)	68,0N	60.0N	34,0N
CS2 HOLD TIME	(TCSH2)	70.0N	62.0N	32.0N
OUTPUT ACTIVE FROM C	SI (TOGAI)	1 . ØØK	236, N	118.N
	S2 (TDOAZ)	268.N	235°N	114.N
OUTPUT ACTIVE FROM M		66.ØN	58.AN	32 QN
OUTPUT HOLD FROM CS1	(TDOH1)	168.N	136, N	46 , ØN
OUTPUT HOLD FROM CS2		164.N	136,N 132,N	
OUTPUT HOLD FROM MRD	•	144 N	135 14	46,0N 36,0N
OUTPUT HOLD FROM MWR		142.N	122, N 120, N	38.0N
READ CYCLE TIME	(TRC)	304,N	256,N	128.N
WRITE CYCLE TIME	(TWC)	272.N	240.N	136.N
IIL	IIH	VICI	Alcs	
AØ #45.3NA	44.8NA	3.42 V	-3,42 V	
A1 -44,9NA	45.8NA	3.46 V	-3,46 V	
A2 =43,2NA	44.4NA	3.50 V	+3,52 V	
A3 =43.8NA	44.3NA	3_49 V	#3.51 V	
A4 #43.2NA	43.0NA	3,46 V	-3,49 V	
A5 =45.5NA	43.8NA	3.39 V	-3,43 V	
A6 -44,4NA	38.4NA	3.45 V	-3,33 V	
A7 -43.9NA	44.5NA	3.43 V	=3.44 V	
CS1 =43,5NA	// // 6 NA	Z EA V	÷3° 47 V	
CS2 -43,9NA	44.6NA 48.5NA	3.50 V 4.28 V	4 / 44 م د ب سیل ۱۳۵۸ کا	
MWR =42,2NA	42.2NA	3.43 V	-4,30 V -3,45 V	
MRD =43.1NA	42.9NA	3.44 V	-3.44 V	
DIØ =43.2NA	AT ELA	2 67 0	la'na u	
DI1 =44,7NA	43.5NA	3,57 V	-3,50 V	
DI2 =41,9NA	42.7NA 42.8NA	3.56 V 3.52 V	-3,50 V -3,48 V	
DI3 =43.5NA	42.9NA	3.46 V	#3,45 V	
	rice at comm	Ja vo v	ты∌ ч э У	

RÇA	CDP182250	256 X 4	CMOS	STATIC	RAM	31	AUG	78	TEMP:	8	3 C
									PAGE	8	OF
	nga	001		Doa	•		po	3			
VOL1	130.MV	135	.MV	149	.MV		14	ν, (ΘΙ			
AOL5	140.MV	145			, MV			ัด MV			
VOH1	4.78 V	4,7	9 V		8 V		4	79 V			
ADHS	9.72 V	9.7	5 A	9.7	'i V		9.	72 V			
IDNi	5.65MA	5.5	ВМА	5.2	ØMA.		5.	30MA			
IDNS	13.8MA	12.	AMP		7MA			AMD.			
IDP1	=1,86MA	-1,8		=1 ₂ 8	6MA		- 1 ·	87MA			
IUP2	₩4.39MA	-4-4	3MA	#4 <u>3</u> 3	AMO		-4	47MA			
IUZ1	195.NA	188	N A	184	.NA		18	8,NA			
Iuza	187 NA	194	NA	180	NA			5 NA			
1023	189.NA	189	NΑ		NA			BANA			
TO24	183 _a NA	196	. N A	181	.NA			S.NV			
1075	187 "NA	195	·ΝΔ	182	NA		18	B.NA			
1026	185.NA	189		192	.NA			6 NA			
IOZI	194.NA	186		187	"NA		18	7 NA			
IOZA	183.NA	197	. N A	183	.NA		18	3 NA			
ILDP	=5.00UA										
IL.1	≖30,0UA										
ILZ	-35.0UA										
113	-25.0UA										
11,4	-50.0AV										

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PAGE 9 0F 10

PASSED	GALPAT	(WIDE	LIMITS)	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS)	VCC=1PV
PASSED	GALPAT	(TIGHT	LIMITS)	VCC=5V

	vcc	= 4.5V	5.0v	10.0V
AUDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA) (TDS) (TDH)	285.N 36,ØN 12.ØN	245'.N 30.0N 12.0N	115.N 10,0N 14.0N
ADDRESS SETUP TIME ADDRESS SETUP TIME ADDRESS HOLD TIME	(TAS1) (TAS2) (TAH)	8.00N 146.N -26.0N	6.00N 130.N -22.0N	4.00N 68.0N -8.00N
WRITE PULSE WINTH	(TWP)	108.N	94 . ØN	52.0N
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(1881) (1882) (1881) (1882)	218.N 214.N 68.0N 72.0N	190, N 184, N 60, ON 62, CN	96,0N 92,0N 34,0N 34,0N
OUTPUT ACTIVE FROM CS OUTPUT ACTIVE FROM MR	(SANGT) Si	288.N 282.N 70.0N	292,N 246.N 62.NN	130.N 128.N 34.0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH1) (TDOH2) (TDOH3) (TPOH) (TRC) (TWC)	170 N 166 N 144 N 146 N 304 N 272 N	138, N 136, N 122, N 122, N 264, N 240, N	50,0N 50,0N 38,0N 40.0N 136.N 144.N
III.	IIH	Aici	VICS	
A0 =263.NA A1 =264.NA A2 =256.NA A3 =254.NA	258, NA 261, NA 257, NA 253, NA	3.47 V 3.51 V 3.56 V 3.54 V	-3,47 V -3,51 V -3,57 V -3,56 V	
	250,NA 256.NA 220.NA 257.NA	3.51 V 3.44 V 3.50 V 3.48 V	-3,54 V -3,48 V -3,36 V -3,50 V	
CS2 =255.NA MWR =247.NA	253.NA 262,NA 244,NA 250.NA	3.55 V 3.56 V 3.48 V 3.49 V	#3,52 V #3,59 V #3,51 V #3.50 V	
DI1 =254.NA DI2 =245.NA	254,NA 250,NA 249,NA 248.NA	3.63 V 3.62 V 3.57 V 3.52 V	=3,56 V =3,55 V =3,53 V ≈3.51 V	

RCA CI	DP18225D	256	X	4	CMOS	STATIC	RAM	31	AUG	78	TEMP:	125	¢	SN:	16
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PAGF 10 OF 10

	000	001	nas	003
VOL 1	145.MV	150.MV	160.MV	155 MV
VOL 2	155.MV	165.MV	185.MV	180 MV
VOH 1	4.76 V	4.76 V	4.76 V	4,76 V
VOH 2	9.68 V	9.68 V	9.67 V	9,68 V
IDN1	5.10MA	4.95MA	4.70MA	4.75MA
IDN2	12.3MA	11.5MA	10.4MA	10.7MA
IDN1	-1.69MA	-1.70MA	-1.66MA	-1.71MA
IDN1	-3.94MA	-3.96MA	-3.84MA	-4.02MA
1021	640.NA	652 NA	654 NA	633, NA
1022	637.NA	643 NA	652 NA	63, NA
1023	630.NA	642 NA	652 NA	630, NA
1024	638.NA	639 NA	649 NA	635, NA
1025	641 NA	647,NA	663.NA	642.NA
1026	636 NA	651,NA	644.NA	644.NA
1027	626 NA	650,NA	649.NA	629.NA
1028	638 NA	641.NA	650.NA	635.NA
ILOP	65. UUA			
IL1 IL2 IL3 IL4	+135.UA -160.UA -120.UA -105.UA			

PAGE 1 OF 10

	E LIMITS) HT LIMITS) HT LIMITS)	VCC=10V VCC=10V VCC=5V	REPRODUCIBILE	TY OF THE
-		A1'C#2A	ORIGINAL PAGE	IS POOR
PASSED DATA RETENTI	UN TEST			
	,	VCC = 4.5V	5.ev	10.0v
ADDRESS ACCESS TIME	(TAA)	240.N	205.N	85,0N
DATA SETUP TIME	(TDS)	26, an	55°ah	8.00
DATA HOLD TIME	(TDH)	19.0N	10.9N	12.NN
ADDRESS SETUP TIME	(TAS1	14.0N	10,AN	4.00N
ADDRESS SETUP TIME	(TAS2	·	98.7N	48. ON
ADDRESS HOLD TIME	(HAT)	=18, ØN	-16.5N	=4.00N
WRITE PULSE WINTH	(TWP)	86.ØN	74,01	40 - 0N
CS: SETUP TIME	(TCSS	1) 182.N	154, N	76,0N
CS2 SETUP TIME	(TCSS	2) 176.N	150.N	74,0N
CS1 HOLD TIME	(TCSH	ľ	50.0N	28,0N
CS2 HOLD TIME	(TCSH	5) 60.0N	52.0N	28.0N
OUTPUT ACTIVE FROM	CS1 (TDOA	1) 232.N	198, N	96,0N
OUTPUT ACTIVE FROM		_	194 N	92,00
OUTPUT ACTIVE FROM	MRD (TDOA)	3) 54.0N	46. AN	88. UN
OUTPUT HOLD FROM CS	1 (TDOH	1) 148.N	118 ₂ N	34,0N
OUTPUT HOLD FROM CS	_		118,N	36,0N
OUTPUT HOLD FROM MR	ואמסד) ט		118, N	34,0N
OUTPUT HOLD FROM MW	R (TPDH') 134.N	114,N	32.ØN
READ CYCLE TIME	(TRC)	≥56.N	216,N	150 N
WRITE CYCLE TIME	(TWC)	256.N	216.N	120.M
IIL	ITH	VIC1	AICS	
A0 -2.80NA	2.70NA	3.19 V	-3,18 V	
A1 -2.70NA	2,70NA	3.23 V	#3,23 V	
45 -5.60N4	2.60NA	3.28 V	=3,28 V	
A3 -2.60N4	2,80NA	3.27 V	-3.27 V	
44 -2,70NA	2,60NA	3,33 V	-3,35 V	
A5 -2,50NA	2,60NA	3.18 V	ლ3,23 V	
A6 =3,00NA	2,4MNA	3.18 V	-3,20 V	
A7 -2.80NA	2.50NA	3'.19 V	=3.19 V	
CS1 -2.70NA	2,50NA	3,27 V	-3,28 V	
CS2 +2,70NA	2.60NA	3.30 V	#3,30 V	
MWR -2.50NA	2,50NA	3.27 V	-5,2/ V	
MRD -2.60NA	2.50NA	3.27 V	-3.28 V	
DIO -2.80N4	2.60NA	3.34 V	-3,24 V -3,23 V	
DI1 +2.50NA	2,60NA	3_28 V	-3,23 V	
DI2 -2.70NA	2,60NA	3.32 V	™3,27 V	
DI3 -2.90NA	2.60NA	3.30 V	-3,25 V	
		B-161		

RCA	CDP18228D	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP:	25 C S
					PAGE	2 OF 10
	nog	001	soa	003		
VOL 1	100,MV	105.MV	115.MV	115, MV		
AOFS	105.MV	120.MV	135 MV	135. MV		
VQH1	4.84 V	4.84 V	4.84 V	4 84 V		
AOHS	9.78 V	9.78 V	9.77 V	4 84 V 9 78 V		
IDN1	7.45MA	7.00MA	6.55MA	6,50MA		
Inn5	17.5MA	15.9MA	14.1MA	14.2MA		
IDPi	-2.49MA	-2,49MA	#2,44MA	∺2 ็น3MA		
1065	#5.61MA	-5.58MA	-5.41MA	+5.53MA		
1071	33.3NA	24.7NA	30,7NA	24,4NA		
1025	31.2NA	24.4NA	31,0NA	23,4NA		
1073	25.5NA	30.6NA	24,7NA	30,4NA		
1174	88.3NA	27.7NA	56_3NA	ANS RE		
1025	29.2NA	26.4NA	30,0NA	24.8NA		
Iuze	89.9NA	26.1NA	29,9NA	24,4N4		
1027	29,9NA	25,9NA	29,9NA 30,0NA	24. 1NA		
IUZ8	30.CNA	25,3NA	30.0NA	24. PNA		
91.55	= +011.					
ILUP	- 5.00U∧					
IL1	-10.0UA					
112	-20,0UA					
ÏL3	-55,0UA					
ÎL4	-50,0UA					
6 to 17	- 141 \$ 611.14					

SN:

PAGE 3 OF 10

PASSED	GALPAT	(WIDE	LIMITS)	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS)	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS)	VCC=5V

	vcc	= 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME DATA SETUP TIME	(TAA) (TDS)	245.N 28.0N	28.0N 200.N	80.0N 8.70N
DATA HOLD TIME	(TDH)	10.0N	10.0N	10.0N
ADDRESS SETUP TIME	(TAS1)	55.0N	16.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	116.N	92. ØN	42.0N
ADDRESS HOLD TIME	(TAH)	-18,0N	=14.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	78.0N	68.0N	38,0N
CS1 SETUP TIME	(TCSS1)	174.N	146 N	70,0N
CS2 SETUP TIME	(Tossa)	172.N	144 N	68,0N
CS1 HOLD TIME	(TCSH1)	46, ØN	40.0N	24,0N
CS2 HOLD TIME	(TCSH2)	46. ØN	38.0N	22.0N
GUARUR LARRIE BALL SOL				a.a.t
OUTPUT ACTIVE FROM CS	· · · · · · · · · · · · · · · · · · ·	226 N	188,N	88, ØN
OUTPUT ACTIVE FROM CS		224 N	186.N	86,0N
OUTPUT ACTIVE FROM MR	(דמממד) מ	48.ØN	42.0N	26.0N
OUTPUT HOLD FROM CS1	(TDOH1)	140 N	110 N	32,0N
OUTPUT HOLD FROM CS2	(SHOOT)	142.N	110,N	34,0N
OUTPUT HOLD FROM MRD	(TDOH3)	138.N	116, N	30,0N
DUTPUT HOLD FROM MWR	(TPDH)	132,N	110,N	30,0N
READ CYCLE TIME	(TRC)	240.N	208 N	120.N
WRITE CYCLE TIME	(TWC)	256.N	224.N	112.N
IIL	IIH	VICI	VICP	
AØ =300 PA	300 PA	3.20 V	-3,19 V	
-	300 PA	3.24 V	-3,24 V	
	300 PA	3.28 V	=3,24 V =3,29 V	
	300 PA	3.28 V	-3.28 V	
			- 1	
	300,PA	3.34 V	-3,35 V -3,24 V	
	300,PA	3.19 V	-3,24 V	
	300,PA	3.19 V	-3,21 V	
A7 #300,PA	300,PA	3.21 V	-3,20 V	
CS1 =300.PA	300.PA	3.28 V	-3,28 V	
	300 PA	3.97 V	-3,96 V	
	200,PA	3,28 V	#3,28 V	
	300.PA	3.28 V	#3,29 V	
DIO =300 .PA	300,04	3.31 V	.3,25 V	
	300.PA	3.29 V	#3,24 V	
	300 PA	3.33 V	43,27 V	
	400 PA	3.31 V	#3,26 V	
	*	D 142		

RCA	CDP1822SD	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP	-50 C	SN:	17
					PAGE	4 OF	10	
	DOW	001	פסס	003				
VOL1 VOL2 VOH1	85.0MV 95.0MV 4.87 V 9.81 V	90.0MV 105.MV 4.87 V	100.MV 115.MV 4.87 V	100 MV 115 MV 4,87 V 9,81 V				
SNGI TNGI SHOV	8.50MA	9.81 V 8.00MA 18.4MA	9.81 V 7.50MA 16.4MA	7.40MA 16.5MA				
IDP1	-2.97MA -6.64MA	-2.94MA -6.64MA	-2.92MA	-2,92MA -6,57MA				
1021 1022 1023 1024	7.60NA	7,70NA 7.10NA 700.PA 2.80NA	1.90NA 700.PA 7.70NA 5.40NA	6,00NA 7,40NA 700,PA 1,90NA			·	
1025 1026 1027 1028	ANDP.S	5,80NA 6,30NA 6,60NA 7,10NA	1.80NA 1.20NA 1.00NA 800.PA	6,80NA 6,90NA 7,40NA 7,50NA				
ILDP	-5.00UA							
IL1 IL3 IL4	⇔5,00UΛ ≈15,0UΛ ≈55,0UΑ ≈50,0UA							

PAGE 5 OF 10

PASSED GALPAT (TIGH	T LIMITS) V	CC=10V CC=10V CC=5V	RÉPRODUCIBILIT GRIGINAL, PAGE	Y OF THE
PASSED DATA RETENTION	N TEST			
	VC	å = 4.5V	5'. @V	10.0V
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA) (TDS) (TDH)	240 N 34 QN 6.004	190.N 24.7N 8.00N	70.0N 8.00N 10.0N
ADDRESS SETUP TIME ADDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WINTH	(TAS1) (TAS2) (TAH) (TWP)	22.0N 112.N -18,0N 80.0N	12.0N .88.0N ~12.0N 66.0N	4.00N 38.0N -2.00N 36.0N
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS1) (TCSS2) (TCSH1) (TCSH2)	166.N 166.N 48.ØN 46.ØN	138,N 138,N 38.AN 38.AN	64.0N 62,0N 22,0N 20,0N
OUTPUT ACTIVE FROM COUTPUT ACTIVE FROM MO	S2 (TODA2)	220.N 216.N 44.0N	178, N 176, N 38, MN	84,0N 82,0N 22.0N
OUTPUT HOLD FROM CS: OUTPUT HOLD FROM CS? OUTPUT HOLD FROM MUR OUTPUT HOLD FROM MUR READ CYCLE TIME WRITE CYCLE TIME	(TDOH1) (TDOH2) (TDOH3) (TPOH) (TRC) (TWC)	134.N 134.N 134.N 132.N 224.N 264.N	104, N 104, N 112, N 108, N 192, N	28,0N 30,0N 38,0N 112,N 112,N
I I I-	IIH	Alui	AICS	
A0 0.00 A A1 =100.PA A2 =100.PA A3 =100.PA	100.PA 0.00 A 100.PA 100.PA	3.23 V 3.27 V 3.31 V 3.31 V	-3,22 V -3,27 V +3,31 V -3,30 V	
AS #100.PA AS #100.PA A6 -100.PA A7 #100.PA	100.PA 100.PA 100.PA 100.PA	3.37 V 3.23 V 3.22 V 3.24 V	=3,37 V =3,27 V =3,25 V =3,24 V	
CS1 0.00 A CS2 0.00 A MWR -100.PA MRD -100.PA	100.PA 100.PA 100.PA 100.PA	3.31 V 3.91 V 3.31 V 3.31 V	-3.31 V -3.91 V -3.30 V -3.32 V	
DIO -100,PA DI1 0.00 A DI2 0.00 A DI3 -100.PA	100.PA 100.PA 100.PA 100.PA	3.35 V 3.31 V 3.36 V 3.34 V	3,28 V +3,27 V +3,30 V +3,28 V	

RCA	CDP1822SD	P56 X 4 CMOS	STATIC RÂM	31 AUG 78 TEMP:	-55 C SN: 17
				PAGE	6 OF 10
	000	100	200	003	•
VOL 1 VOL 2 VOH 1	4.88 V	85.0MV 90.0MV 4.89 V 9.84 V	90'.0MV 105.MV 4.88 V 9.84 V	90.0MV 100.MV 4,89 V 9.84 V	

IDN1	9.35MA	8.85MA	8.30MA	8,50MY
IDN2	2ã.4M∧	20.6MA	18 4MA	18.4MA
IDPI	-3 44MA	-3.46MA	-3.40MA	-3,39MA
IUPZ	-7.68MA	-7.70MA	-7.47MA	-7 -61 MA
IOZ1	3,20NA	2,00NA	1.10NA	2.50NA
1025	6.10NA	-1,30NA	4.80NA	-900 PA
1023	-1.10NA	5,10NA	-1.10NA	4,40NA
1074	-500.PA	3.90NA	=1.20NA	4.70NA
tozs	4.50NA	-1.30NA	5,00NA	₩2°00NV
1076	4,60NA	-1.50NA	4.60NA	-1,70NA
1077	4.20NA	-1,10NA	4.60NA	-1.80NA
IUZ8	4.30NA	-1.20NA	4 . 40NA	-1.69NA

ILDP	∾5.00UA
ILi	⇔5,00UA
ILS	-15.6UA
113	-55, ØUA
IL4	-55.QUA

	<u> </u>	¥	e e	
			_	
RCA CDP182250 256 X 4	CMOS STAT	IC RAM 31	L AUG 78 TEMP	85 C SN:
			_	
			PAGE	7 OF 10
PASSED GALPAT (WIDE L	.IMITS) VCC	4.5.U		
		=10V =10V		
PASSEU GALPAT (TIGHT L	•			
Section of Application of Application of	2	- 7 4		
PASSED NATA RETENTION	TEST			
	VCC :	= 4.57	5.0V	10.0V
			, t ,	· ·
ADDRESS ACCESS TIME	(TAA)	240 N	ato'N	95. ØN
DATA SETUP TIME	(TDS)	28,0N	24.0N	8 • 00 M
DATA HOLD TIME	(TDH)	12.9N	12.0N	12.0N
ADDRESS SETUP TIME	(TAS1)	8.00N	8.00N	4.90N
ADDRESS SETUP TIME	(TAS2)	155 N	108 N	56.0N
ADDRESS HOLD TIME	(YAH)	-18.0N	-16.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	100.N	86. MN	48.0N
			_	_ ,
CS1 SETUP TIME	(TCSS1)	192.N	166, N	86,0N
CSS SETUP TIME	(TCSS2)	188_N	162.N	85,0N
CS1 HOLD TIME	(TOSH1)	66,0N	58.0N	34,0N
CS2 HOLD TIME	(TCSH2)	70.0N	60.0N	32.0N
BURBUT LOSTUM MOGULAGA				
OUTPUT ACTIVE FROM CS1	(TDOA1)	242.N	212,N	110.N
OUTPUT ACTIVE FROM CS2	(SAOGT)	236.N	208.0	106.N
OUTPUT ACTIVE FROM MRD	(TDDA3)	58.0N	52.0N	30.0N
OUTPUT HOLD FROM CS1	(TDOH1)	154.N	124 N	38,0N
OUTPUT HOLD FROM CS2	(SHOOT)	152.N	iža,	40,0N
OUTPUT HOLD FROM MRD	(TDOH3)	140.N	118.N	36, ØN
OUTPUT HOLD FROM MWR	(TPDH)	138 N	116,N	36.2N
READ CYCLE TIME	(TRC)	272.N	232 N	128.N
WRITE CYCLE TIME	(TWC)	756 N	224.N	136.N
·	- · · · ·		- · · · · · · · · · · · · · · · · · · ·	•

	IIL	IIH	VIC1	vica
AØ	=42.1NA	41.1NA	3.20 V	+3,19 V
Ai	-42,0NA	41.3NA	3,24 V	±3,25 V
A 2	41,6NA	40.6NA	3.30 V	-3,30 V
ΣA	=41 QNA	41.5NA	3.29 V	≈3.29 V
A 4	-41.1NA	40.0NA	3.36 V	-3,37 V
A5	-41.4NA	41.0NA	3.20 V	-3,24 V
A 6	-42.7NA	39.5NA	3.19 V	-3,24 V
A7	#42,1NA	41,0NA	3.21 V	-3.21 V
CSI	-41,0NA	A 49. 9E	3'.29 V	-3,29 V
csa	-41.2NA	42,1NA	3.31 V	∞3.33 V
MWR	-40.0NA	39.4NA	3.29 V	-3,28 V
MRD	#41 1 NA	39.5NA	3.29 V	-3.30 V
DIO	-40,6NA	40.7NA	3.32 V	=3,26 V
DII	-39,9NA	41.1NA	3.29 V	=3,25 V
DIS	-41 6NA	40.8NA	3.34 V	-3.28 V
013	-40.7NA	40.6NA	3.32 V	-3.27 V
			B-167	

RCA	CDP182250	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP	85 C SN:
					PAGE	8 OF 10
	DOM	DO1	saa	003		
VOLI	115.MV	125.MV	135.MV	135, MV		
VOL 2	130 MV	140 MV	160 MV	160 MV		
VOH1	4.82 V	4,81 V	4.80 V	4 80 V		
VUHS	9.73 V	9.73 V	9.72 V	160 MV 4,80 V 9,73 V		
IDN1	6.35MA	6.00MA	5.55MA	5.55MA		
IDNS	14,8MA	13.5MA	11.9MA	12.1MA		
IDP1	-2.10MA	-2,08MA	-2.03MA	#2,06MA		
1065	-4.70MA	-4.68MA	≈4.53MA	-4.65MA		
TOZI	271.NA	273,NA	565°NY	250, NA		
1025		266,NA	566*NY	244, NA		
1023		268,NA	263 NA	246,NA		
1024	270.NA	265.NA	269.NA	244.NA		
1025	88.9 , NA	268, NA	271.NA	250,NA		
IOZ6	AM.EBS	264 NA	267.NA	255,NA		
1027	271 NA	274,NA	260 NA	254 NA		
1078	273.NA	264.NA	273.NA	246.NA		
ILDP	1.80UA					
dy has had for	TONDA					
ILI	-35.0UA					
115	-50.0UA					
IL3	-75,0UA					
IL4	-70 0UA					

PASSED PASSED PASSED	GALPAT	(TIGHT	LIMITS) LIMITS) LIMITS)	VCC=10V VCC=10V VCC=5V
PASSED	DATA RE	TENTION	TEST	

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOK

PASSED	DATA	RETENTION	TEST

PASSED DATA RETENTION '	TEST		Name .	
	vcc	= 4.5V	5. av	10.0V
ADDRESS ACCESS TIME	(TAA)	255.N	225 N	110.N
DATA SETUP TIME	(TDS)	28, ØN	24. ON	10,0N
DATA HOLD TIME	(TDH)	14.0N	14.0N	14 ØN
DHIM HOLD IIII	(1511)	1 7 8 50 17	T - S Hits	*
ADDRESS SETUP TIME	(TAS1)	6.00N	4.ื่อดูก	4.000
ADDRESS SETUP TIME	(TAS2)	132.N	118 N	64, ØN
ADDRESS HOLD TIME	(TAH)	-20'0N	-18 -7N	-6.00N
WRITE PULSE WIDTH	(TWP)	104.N	92. AN	52.ØN
CS1 SETUP TIME	(TCSS1)	206.N	180', N	94, ON
CS2 SETUP TIME	(TCSS2)	202.N	174.N	90,0N
CS1 HOLD TIME	(TCSH1)	68.0N	62. ØN	34,0N
CS2 HOLD TIME	(TCSH2)	72.ØN	68. MN	34.0N
			,	
OUTPUT ACTIVE FROM CS1	-	258 N	230°N	122.N
OUTPUT ACTIVE FROM CS2		254.N	224.N	118.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	62.ØN	56.AN	34.0N
AUTOUS DOUB SOOM ASA	6700U43	4 / CL N	430 1	44. ØN
OUTPUT HOLD FROM CS1	(TDOH1)	160 N	128 N	ľ
OUTPUT HOLD FROM CS2	(T00H2)	156.N	126,N	44,0N
OUTPUT HOLD FROM MRD	(TDOH3)	142.N	125 N	38,0N
DUTPUT HOLD FROM MWR	(TPDH)	142,N	118,N	40.0N
READ CYCLE TIME	(TRC)	280 N	248 N	128.N
WRITE CYCLE TIME	(TWC)	264.N	240 N	144 N
11r I	IH	VIC1	VTCP	
AØ =243.NA 2	34.NA	3.24 V	-3,29 V	
	36,NA	3.29 V	-3.29 V	
	32,NA	3.35 V	-3,35 V	
	33.NA	3.33 V	+3,35 V +3,34 V	
	,		~ 1	
	27,NA	3.40 V	-3,41 V	
· · · · · · · · · · · · · · · · · · ·	34.NA	3.23 V	≖3,29 V	
	27,NA	3.23 V	#3,26 V #3.25 V	
A7 -241.NA 2	33.NA	3,25 V	#3.25 V	
	26, NA	3.34 V	-3,34 V	
CSS +536*NV 5.	34, NA	3,37 V	=3,38 V	
	23,NA	3.34 V	5,34 V	
MRD #233.NA 2.	25.NA	3.34 V	-3.35 V	
010 =232.NA 2	31.NA	3.37 V	-3,30 V	
	31.NA	3.34 V	-3,29 V	
	32.NA	3.38 V	+3,33 V	
-	28.NA	3.37 V	-3.31 V	
we war = 111	· · · · · · · · · · · · · · · · · · ·			

RCA	CDP1822SD	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP	125 C	SN:	17
					PAGE	10 OF	10	
	000	001	005	pa3				
00H5 0H7 0F7	130.MV 145.MV 4.79 V 9.70 V	140.MV 160.MV 4.78 V 9.69 V	155.MV 180.MV 4.78 V 9.69 V	150 MV 180 MV 4,78 V 9,69 V				
IDN1 IDN2 IDP1 IDP2	5.65MA 13.1MA -1.88MA -4.20MA	5.35MA 11.9MA -1.86MA -4.18MA	4.95MA 10.6MA -1.82MA -4.03MA	4,95MA 10,7MA -1,84MA -4,16MA				
1021 1022 1023 1024	1.09UA 1.09UA 1.08UA 1.07UA	1,06UA 1,05UA 1,06UA 1.06UA	1.03UA 1.04UA 1.03UA 1.03UA	995, NA 990, NA 984, NA 992. NA				
1075 1076 1077 1078	1.10UA 1.09UA 1.08UA 1.08UA	1.06UA 1.06UA 1.05UA 1.05UA	1 .04UA 1 .04UA 1 .04UA 1 .04UA	995, NA 989, NA 988, NA 987, NA				
ĭĻnp	70.0UA							
IL1 IL2 IL3 IL4	-130.UA -160.UA -170.UA -150.UA							

RCA CDP1822SD 256	X 4 CMOS STA	TIC RAM 31	L AUG 78 TEMP:	25 C SN:
			PAGE	1 OF 10
PASSED GALPAT (WIDE	LIMITS) VO	:C=10V		
PASSED GALPAT (TIGH		C=10V		
FAILFD GALPAT (TIGH	T LIMITS) VO	CC=5V ADD	= 56 DIAG =	9 PIN: 010
PASSED DATA RETENTIO	N TEST			
	64.00.00		Pr. * #444	ta' au
	VET	: = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	450.N	330.N	105 N
DATA SETUP TIME	(TDS)	20,0N	18.0N	8.00k
DATA HOLD TIME	(* 0#)	12.ØN	12.0N	12.0N
ADDRESS SETUP TIME	(TAS1)	8.00N	8 . ØØN	4 . 00N
ADDRESS SETUP TIME ADDRESS HOLD TIME	(TAS2)	242.N	184 N	54.0N
WRITE PULSE WIDTH	(TAH) (TWP)	-14.0N 70.0N	-12.0N 60.0N	-2.00N 36.0N
MATIE LATSE MIDIO	(IME)	/Wa Wild	-	N
CS: SETUR TIME	(TCSS1)	372.N	1.00K	418.N
CS2 SETUP TIME	(TCSS2)	294 N	142.N	68, ØN
CS1 HOLD TIME CS2 HOLD TIME	(TCSH1) (TCSH2)	38,0N 40.0N	32.0N	24,0N
COS HOLD TIME	(Tubne)	40.04	34.AN	55.0N
OUTPUT ACTIVE FROM C		414.N	318, N	114.N
OUTPUT ACTIVE FROM C		410 N	314.N	112.N
OUTPUT ACTIVE FROM M	RD (TDGA3)	54.0N	4R. ØN	26,0N
OUTPUT HOLD FROM CS1	(TDOH1)	154.N	122,N	36, ØN
DUTPUT HOLD FROM CS2	(TDOH2)	150.N	118 N	36,0N
OUTPUT HOLD FROM MRD	(TDOH3)	142 N	120 N 114 N 312 N	34,0N
OUTPUT HOLD FROM MWR READ CYCLE TIME	(TPOH) (TRC)	140.N	114 N	32.0N
WRITE CYCLE TIME	(TWC)	392.N 208.N	184.N	120.N 112.N
	·			126 81
IIL	IIH	VIC1	VTCE	
ANNS.S- DA	2,20NA	2.94 V	-2,93 V	
A1 =1.80NA	2.10NA	2.97 V	-3,00 V	
AZ -2. PØNA	2,30NA	3.01 V	-3,01 V	
A3 -1.90NA	2.40NA	3.01 V	-3.03 V	
A4 -1.88NA	2,00NA	3.01 V	-3,02 V	
A5 -2.10NA	2.00NA	2.93 V	42,98 V	
A6 =2.00NA A7 =2.50NA	2,30NA	2.90 V	-2,96 V	
A7 -2,50NA	2.60NA	2.94 V	-2.97 V	
CS1 -2.00NA	2.70NA	2.99 V	÷2,98 V	•
CS2 -2,30NA	2.40NA	3.02 V	∞3,04 V	
MWR =2.00NA MRO =2.10NA	2,10NA 2,60NA	2,93 V 2,95 V	#2,96 V #2,95 V	
-				
010 +2.50NA	2,50NA	3.09 V	-3,04 V	
DI1 =2,40NA	2,80NA	3.07 V	-3,02 V	
DI2 =2.60NA DI3 =2.70NA	2.60NA	3.07 V 3.05 V	%3,03 V ≈3,03 V	
OF3 -CALMAN	E ● O AMA W	א ריאי≇ני	Ma_wa V	

RÇA	CDP182280	256 X 4 Ch	MOS STATIC R	AM 31 AUG	78 TEMP:
					PAGE
	Dog	100	200	D	03
VOLI	115.MV	115 M		MV 1	25 , MV
AOLS	110.MV	120.41		MV 1	30.MV
VOHI	4.86 V	4,85 \	4.85	v 4	30 MV 86 V
VOHS	9.79 V	9.78		5 V 9'	.79 V
IONI	6.35MA	6'.15M/	5.85	MA 5	90MA
IDNS	16.8MA	15,74/			4.5MA
IDP1	-2.64MA	-2,62M/		MA -2	64MA
IDES	-5. 82MA	-5.82 M	45.68	IMA =5	# BBMA
IOZ1	28,5NA	27.0N/		INA 3	4.5NA
IOZS	30,2NA	23.6N/		'NA 3	1.BNA
1023	31,2NA	21.4N/	30,3	ina 2	7.5NA
1074	28.3NA	24.7N	27'.4	INA 3	A.SNA
1925	31.8NA	21.90/		INA 3	21,3NA
1026	31,5NA	55"2V	7 ۾ 88	'NA 31	7.7NA
1027	31,1NA	22.3NA	1 28,2	NA 31	7 . 7 N A
1028	30.4NA	22.8NA	N 27 <u>.</u> 9	NA 3	7.BNA
ILDP	AU00.5				
141	≈200ªUV				
ILZ	⇔200.UA				
IL3	⇔≳0,gUA				
IL4	=15.0UA				

25 C

2 OF 10

SN:

RCA CDP182280 256	X 4 CMOS STA	TIC RAM 31	AUG 78 TEMP:	#20 C SN:
			PAGE	3 OF 10
PASSED GALPAT (WIDE	E LIMITS) VO	:C=10V		
		C#10V C#5V ADD	= 8 DIAG =	9 PIN: 010
· · · ·				
FAILED DATA - 'SNTIC	N TEST ADD ≈	97 DIAG		
	VCC	: = 4.5V	s . øv	10'. 0V
AUDRESS ACCESS TIME	(TAA)	535.N	370 N	100.N
DATA SETUP TIME DATA HOLD TIME	(TDS) (Toh)	32,0N 10,0N	18,0N 10,0N	8.90N 10.0N
ADDRESS SETUP TIME	(TAS1)	42.0N	10.QN	4 - UON
ADDRESS SETUP TIME	(TAS2)	278.N	194.N	50,0N
ADDRESS HOLD TIME WRITE PULSE WIDTH	(TAH) (TWP)	=16.0N	#12.0N	-2.00N
Muric LACSE Minita	(IME)	68.ØN	58.0N	36.0N
CS1 SETUP TIME	(TCSS1)	402.N	506 N	66, ØN
CS2 SETUP TIME CS1 HOLD TIME	(TCSS2) (TCSH1)	366.N	200'N 34.0N	62,0N
CS1 HOLD TIME CS2 HOLD TIME	(TCSH2)	38,0N 40,0N	34.0N	22.0N 22.0N
	g , m m . (m 2			
OUTPUT ACTIVE FROM (1.00K	342 N	110.N
OUTPUT ACTIVE FROM (1.00K	338.N	106.N
OUTPUT ACTIVE FROM A	RD (TDOA3)	50.0N	AH BN	24.0N
OUTPUT HOLD FROM CS:	(TD0H1)	146.N	114 N	34, an
OUTPUT HOLD FROM CS		144 _n N	112,N	34 P Ø N
OUTPUT HOLD FROM MRC		140.N	116 N	30,0N
OUTPUT HOLD FROM MWF		1,00K	114,N	32.0N
READ CYCLE TIME	(TRC)	400 N	312,N	112.N
WRITE CYCLE TIME	(TWC)	208_N	176.N	104.N
IIL.	11H	Alcı	AICS	
400 -400 PA	300,PA	3.05 V	-3,03 V	
A1 -300.PA	300 PA	3.08 V	-3,10 V -3,11 V	
A2 -400.PA	400°PA	3.12 V	۷ 11 م a a .	
A3 =300,PA	400.PA	3.12 V	∞3,13 V	
A4 =300.PA	200, PA	3.12 V	#3,12 V	
A5 -400.PA	300 PA	3.03 V	-3,08 V	
A6 =300.PA	300,PA	3.00 V	-3 07 V	
A7 '=500.PA	400.PA	3.04 V	=3.07 V	
CS1 -300.PA	400 PA	3.10 V	+3,09 V	
CS2 =400,PA	400,PA	3.12 V	#3,13 V	
MWR -300.PA	300.PA	3.03 V	=3,06 V	
MRD #300.PA	500.PA	3.06 V	=3.05 V	

DIB

DII

012 013 -400.PA

-500.PA

3.18 V 3.17 V 3.16 V 3.15 V *3,13 V *3,12 V *3,13 V *3,13 V

400.PA 400.PA 500.PA 400.PA

RCA	CDP182250	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP	⇒50 C	SN:
					PAGE	4 OF	10
	000	DOI	002	003			
VOLI	105.MV	105.MV	110.MV	110 MV			
AOUS	95.0MV	105.MV	115.MV	115.MV			
VOH	4.88 V	4,88 V	4.88 V	4,88 V 9.82 V			
V0H5	9.82 V	9.82 V	9.82 V	9.82 V			
IDN1	7.10MA	6,90MA	6.55MA	6.65MA			
IDNS	19.3MA	18.1MA	16.3MA	16.7MA			
IDP1	₩3,09MA	⇔3. 08MA	-3.06MA	-3,10MA			
IOP2	⇔6.86MA	+6.86MA	=6.77MA	-6.94MA			
1021	7.80NA	3,30NA	5.90NA	4,70NA			
IOZ2	9,2004	1.30NA	8.70NA	1,90NA			
IOZ3	2,20NA	8,30NA	1,50NA	8,20NA			
1024	4 . 00NA	6.40NA	1.80NA	7,50NA			•
1025	7.80NA	1,50NA	7.60NA	1,80NA			
1026	7.80NA	1,50NA	7.90NA	1,30NA			
1027	8,00NA	1,20NA	7.70NA	1,70NA			
1028	8.1@NA	1,40NA	8.00NA	1.60NA			
ILDP	-5.00UA						
	*** * ** * ** *						
IL1	∞205.UA						
ILS	AU, DOS-						
11.3	-10.0UA						
IL4	-5.00UA						
	- -···						

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RCA	CDP18	32251	, יו	256	X	4	Ch	105	§ S	TA	TIC	: F	MAS	3	1	AUG	7	8	T	Емр:	es 5	55	C	SN:	1 8
																			F	PAGE	ç	5 0	F 1	7	
PASSE	D GAL	PAT	()	v I D I	Ē	LI	MIT	'S 1		۷C	C = 1	ดน	1												
PASSE				IIG																					
FAILP	D GAL	PAT		ΓIG							C=9			ADD	2		6	DIA	ł G	5	9	PI	Ni	210	
FAILE	TAD O	A RI	ETEN	JT I	QΝ	TE:	S T	٨	ממו	2		97	ט י	TAG	2	,	17	PIN	:	010					
									٧	СC	=	4.	5 V				5	•0V			1	0.	۵v		
ADDRE	SS AC	CES	S T	(ME			(7	ΑΑ	1)			1.	, g g l	ĸ			41	ar'n	N		ç	15.	ØN		
DATA							(1	DS)			26	. 01	N			2	ด "ดง	Ú		P	. 🕝	Ø NI		
DATA	HULL	TIM	F				(1	IJΗ	1)			8.	901	И				. ይወለ				0			
	SS 58								1)				2.				8	" u u V	v			. 0			
	SS SE								5)				001					14.N				8.			
	\$5 HO							AH					ØØI			•		5. MN				.0			
WRITE				•			(F	WP)			68	. 01	¥				0.0N				2.			
	SETUP						(T	C S	51)		48	4.1	V			5.	30, N	į		6	2,1	ŻΝ		
	SETHP								SP				0					28 N			6	0,1	M		
	HOLD								H1				991					a on			- 2	2,1] N		
685	носо	1 T	15				(T	CS	H5)		1.	OOF	<			3 (6.7AN	}		5	2.	ን ሶ		
OUTPU									A 1			١.	OBH	(36	64 N	ı		1	Ø4.	N		
อมรคบ												1.	MAR	<			36	62. N	ł		1	02.	N		
OUTPU	T ACT	TVE	FRO	M N	4RD		(T	סט	Α3)		48	.01	J				7 . 0 N			ج	4 . (2N		
OUTPU									Н1				o gr				1 1	10,0	ł		3	ء زج	ðN!		
OUTPU	T HOL	በ ምክ	MUS	CSa	2		T						904				10	78 N	;		3	2,0	ΝĘ		
OUTPI	T HUL.	D FF	₹∏M	MR)				H3	}			004				1 '	16, N	į		3	Ø , (M		
DUTPH				МЫР	4		(T						001				11	12,N 18,N				0.0			
READ)				١, ح				3	28 N				24			
WRITE			· ME				LI	W C	.)			ہے تی	4.	N]			1	76.N	I		9	6.0	ð N		
	II	L			I	ΙH					۷I	Ci					Ca								
ΔØ	-10	0.P/	7		1	øø,	P A				3.	14	٧			-3,	. 1 7	۶ v							
A1		Ø.PA			1	αu,	PΑ				3.	17	٧			-3,	.19	9 V							
A 2		ព				aa,							٧			-3,									
A 3	⇔ 1 Ø	Ø.PA	١		1	96	, P ∆				3.	71	٧			-3.									
Δ4	-10	0.PA	1		1	п 0,	PA				3.	20	٧			-3,	21	L V	i	WEID-					
A 5		n,pA			1	øø,	PA				3.	12	٧			-3 ,	17	7 V		TA NO	DU	CD_{0}	>-		
A6		O.PA				ØИ,					3.					- 3,			•	ALIGN.	۸ř.		u_{lT}	YOR	 .
Δ7	-1 0	M.PV			1	90.	PA				3.	13	٧			⇒3 ′,	16	5 V			-	#.A	GE j	Y OF 1	HE
CS1		O.PA				aa.					3.					-3,	17	7 V							•
csa		O.PA				ØЙ,					3.					-3.	22	, A							
MWR		Ø.PA				00,					3.					-3,									
MRD	-10	01 , P A	ŀ		1	00.	, PA				3.	16	٧			-3.	-								
DIO		Ø.PA			1	aa.	PA				3.	28	٧			-3	22	, A							
DII		0.PA				90.					3.	26	٧			-3									
uis		Ø,PA				70,					3.	25	٧			-3.	21	V							
013	≈ 10	Ø.PA	١		1	ØØ.	PA				3.	24	٧			-3.									

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RCA	CDF1822SD	256 X 4 CMDS	STATIC RAM	31 AUG 78	TEMP:	955 C SN;	1
					PAGE	6 OF 10	
	DOM	001	200	003			
AOH5 AOH1 AOF5	95.0MV 85.0MV 4.89 V 9.84 V	95,0MV 95,0MV 4,89 V 9.84 V	100.MV 105.MV 4.89 V 9.84 V	100, MV 100, MV 4,89 V 9,85 V			
ION1 IOP1 IOP2	7.75MA 21.3MA -3.51MA -7.87MA	7.50MA 20.0MA -3.53MA -7.91MA	7.15MA 18.2MA #3.53MA #7.74MA	7.20MA 15.6MA #3,56MA #8.01MA			
1021 1022 1023 1024	3,60NA PA 9,002 5,20NA 5,20NA	800.PA 4.50NA -400.PA -1.30NA	3.50NA -400.PA 4.00NA 5.20NA	-100.PA 3.90NA 300.PA -1.60NA			
1025 1026 1027 1028	-800.PA +800.PA +500.PA +500.PA	5,20NA 5,00NA 5,00NA 4,80NA	-1.60NA -1.50NA -1.60NA -1.40NA	5,50NA 5,60NA 5,30NA 5,30NA			

ILDP	1,2001
ILi	-215.UA
IT5	-210.UA
IL3	-5.00UA
TL, 4	+5.00HA

RÇA	CDP1822SD	256 X 4	CMOS	STATIC	RAM	31	AUG	78	TEMP:	85 C	SN:	18
									PAGE	7 NF	10	

			PA	GF 7 OF 10
PASSED GALPAT (TIGH	T LIMITS) VC	C*10V C=10V C=5V ADD	m P4 DIAG =	121 PTN: 010
FAILED DATA RETENTION	N TEST ADD =	97 DTAG	# 17 PIN:	Ø10
	VCC	s 4.5V	5'.0v	10.00
ADDRESS ACCESS TIME	(TAA)	405.N	310 N	145N
DATA SETUP TIME	(TDS)	20,0N	18.0N	800N
DATA HOLD TIME	(TDH)	14.0N	14.0N	140%
ADDRESS SETUP TIME	(TAS1)	4.00N	4.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	226.N	178.N	58.0N
ADDRESS HOLD TIME	(TAH)	-14,0N	-10.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	78.0N	70.0N	42.0N
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS1)	230.N	146' N	78' ØN
	(TCSS2)	226.N	142' N	76' ØN
	(TCSH1)	48.MN	44' ON	28' ØN
	(TCSH2)	52.DN	46' ON	28' ØN
OUTPUT ACTIVE FROM COUTPUT ACTIVE FROM COUTPUT ACTIVE FROM MI	SE (TDOAE)	384.N 380.N 58.0N	306 N 304 N 50 ON	154.N 152.N 30.0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH1)	156, N	124, N	38,0N
	(TDOH2)	154, N	122, N	38,0N
	(TDOH3)	142, N	122, N	36,0N
	(TPOH)	142, N	116, N	1,00K
	(TRC)	400, N	320, N	168,N
	(TWC)	216, N	200, N	128,N
īIL	ITH	VIC1	vice	
A0 -26.1NA	27.2NA	2.89 V	-2.87 V	
A1 -24,3NA	26.0NA	2.91 V	-2.93 V	
A2 -25.5NA	27.8NA	2.95 V	-2.95 V	
A3 -24,7NA	26.9NA	2.95 V	-2.98 V	
A4 -24.5NA	25.9NA	2.95 V	#2,96 V	
-25.7NA	26.6NA	2.87 V	#2,91 V	
A6 -25.0NA	27.2NA	2.84 V	#2,91 V	
A7 -26.6NA	28.9NA	2.88 V	#2,91 V	
CS1 -26,0NA	28.4NA	2.93 V	=2,93 V	
CS2 -26,1NA	28.0NA	2.95 V	=2,97 V	
MNR -25,0NA	26.8NA	2.86 V	=2,91 V	
MRD -26,4NA	28.1NA	2.89 V	=2.89 V	
DIØ -27,4NA	28.7NA	3.03 V	=2,98 V	
DII -27,5NA	29.8NA	3.01 V	=2,96 V	
DI2 -27,5NA	29.1NA	3.01 V	=2.97 V	
DI3 -27,5NA	28.0NA	3.00 V	=2.97 V	

RCA	CDP1822SD	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP:	85 C SN:	18
					PAGE	8 OF 10	
	DDØ	001	soo	003			
00H2 VOH1 VOL1	130.MV 130.MV 4.82 V 9.74 V	135,MV 140.MV 4,82 V 9,75 V	145.MV 160.MV 4.82 V 9.74 V	145 MV 155 MV 4,82 V 9,74 V			
ION1 ION2 IOP1 IOP2	5.55MA 14.3MA -2.23MA -4.92MA	5,35MA 13,3MA =2,21MA =4,91MA	5.10MA 11.9MA -2.21MA -4.82MA	5'.15MA 12.3MA -2,23MA -4.97MA			
1071 1073 1074	223.NA 218.NA 210.NA 210.NA	128,NA 122,NA 117,NA 121.NA	206.NA 198.NA 198.NA 190.NA	209,NA 211,NA 205,NA 212.NA			
1025 1026 1027 1028	211.NA 205.NA 208.NA 208.NA	119.NA 131.NA 119.NA 119.NA	196,NA 190,NA 201,NA 193,NA	211,NA 211,NA 203,NA 215.NA			
ILDP	15.0UA						
IL1 IL3 IL4	#220.UA #230.UA #55.0UA #45.0UA						

FAGE 7 1/1 17.	Р	Αt	36		9	O	F	1	0
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FAILED	GALPAT	(WIDE	LIMITS)	VCC≈10V	ADD	2	82	DIAG	=	64	PIN:	0.10
FAILED	GALPAT	(TIGHT	LIMITS)	VCC=10V	ADD	t	83	DTAG	22	64	PIN:	010
FAILED	GALPAT	(TIGHT	LIMITS)	VCC=5V	ADD	2	8	DIAG	50	12 i	PIN:	010

		and the second s				•	
CATICAN	/\ \ = 1	- 本にせているてった	TECT	* L/ L/	AT BELL A	**************************************	PA # P3
CAILLI	17414	12 P 1 P 19 1 1 1 1 1 1 1 1 1 1	1631	A()() =	97 DIAG 2	17 PTN:	U1 1 U1
				74 P 11	,, ,, ,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,		

	VC	C = 4.5V	5 . / 0 V	10.0V
ADDRESS ACCESS TIME	(TAA)	420.N	325'N	1.00K
DATA SETUP TIME	(TOS)	20,0N	18.0N	1.00K
DATA HOLD TIME	(TDH)	16.0N	16.0N	1.00K
ADDRESS SETUP TIME	(TAS1)	2.00N	2.00N	1.00K
ADDRESS SETUP TIME	(TAS2)	234.N	182'N	64,0N
ADDRESS HOLD TIME	(TAH)	-12.0N	=10.0N	1.00K
WRITE PULSE WIDTH	(TWP)	84.0N	76.0N	1.00K
CS1 SETUP TIME CS2 SFTUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS1)	244 N	158,N	1.00k
	(TCSS2)	244 N	154,N	1.00k
	(TCSH1)	50,0N	46,MN	1.00k
	(TCSH2)	54.0N	48,MN	1.00k
OUTPUT ACTIVE FROM OUTPUT ACTIVE FROM OUTPUT ACTIVE FROM	CS1 (TDDA1)	408.N	328, N	1.00K
	CS2 (TDOA2)	406.N	324, N	1.00K
	MRD (TDOA3)	62.0N	54, MN	1.00K
OUTPUT HOLD FROM CS OUTPUT HOLD FROM MR OUTPUT HOLD FROM MR READ CYCLE TIME WRITE CYCLE TIME	(TD0H2)	162.N 156.N 144.N 144.N 432.N 216.N	130, N 126, N 122, N 120, N 336, N 216. N	1.00K 1.00K 1.00K 1.00K
116	IIH	VICI	AICS	
A0 =148.NA	146 NA	2.84 V	-2'83 V	

	JIL.	ITH	VICI	ATCS
AØ	-148.NA	146.NA	2.84 V	-2',83 V
Ai	-143.NA	142,NA	2.87 V	-5,84 A
A2	-147.NA	148, NA	2.91 V	-2,92 V
A 3	=145.NA	145.NA	2.91 V	#2,94 V
A 4	#141 NA	140.NA	2.91 V	=2,93 V
A5	≈146.NA	142.NA	2.83 V	⇔2jeA V
A6	-147,NA	142,NA	2.79 V	\$2,87 V
47	-148.NA	143.NA	2.84 V	-2.87 V
CS1	=151.NA	144.NA	2.89 V	-2,89 V
csa	=145.NA	146.NA	2.92 V	-2,94 V
MWR	=141.NA	143,NA	2.81 V	-2,87 V
MRD	-144.NA	145 NA	2.84 V	-2.86 V
010	-942.NA	142.NA	2.99 V	-2'94 V
DII	= 143.NA	143.NA	2.97 V	-2,94 V -2,93 V
012	-142.NA	139,NA	2.97 V	2,94 V
013	=141.NA	139.NA	2.96 V	-2.93 V

KUA	COP182280	256 X 4 CMOS	STATIC RAM	51 AUG 78	L F W H T
					PAGE
	DOØ	001	200	003	
VOL 2 VOH 1 VOH 2	145.MV 150.MV 4.80 V 9.72 V	155,MV 160.MV 4.80 V 9.72 V	160.MV 180.MV 4.80 V 9.70 V	160 MV 175 MV 4 80 V 9 72 V	
ION1 ION2 IOP1 IOP2	5.00MA 12.7MA ~2.02MA ~4.43MA	4.85ma 11.9ma -2.00ma -4.40ma	4.55MA 10.6MA +1.99MA +4.33MA	4.65MA 11.0MA -2.02MA -4.47MA	
1071 1022 1023 1024	680.NA 647.NA 641.NA 631.NA	294.NA 281.NA 270.NA 272.NA	594.NA 578.NA 580.NA 572.NA	667,NA 673,NA 667,NA 667,NA	
1025 1076 1027 1028	644.NA 636.NA 632.NA 636.NA	279,NA 287.NA 275.NA 275.NA	595.NA 585.NA 598.NA 583.NA	679, NA 675, NA 671, NA 675, NA	
ILDP	75.0UA				
IL1 IL2 IL3 IL4	-330.UA -370.UA -180,UA -145.UA			•	

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RCA CDP1822SD 256 X	4 CMOS STA	TIC RAM 31	AUG 78 TEMP:	25 C 8N:
			PAGF	1 OF 10
	'LIMITS) VC		200 DIAG =	57 PTN: 010
PASSED DATA RETENTION	TEST			
	vcc	= 4.5V	5 ๎ูด∨	10°0V
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA)	410.N	315'.N	105.N
	(TDS)	24.0N	20.0N	8.00N
	(TDH)	12.0N	12.0N	12.0N
ADDRESS SETUP TIME	(TAS1)	16.0N	14.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	234.N	182.N	58.0N
ADDRESS HOLD TIME	(TAH)	-20,0N	-16.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	76.0N	64.0N	38.0N
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS1)	252.N	154 N	76,0N
	(TCSS2)	248.N	150 N	72,0N
	(TCSH1)	36.0N	32 ON	22,0N
	(TCSH2)	40.0N	36 ON	22.0N
OUTPUT ACTIVE FROM CS OUTPUT ACTIVE FROM CS OUTPUT ACTIVE FROM ME	(1AOOT) 18 (SAOOT) SE	386.N 384.N 56.0N	304, N 302. N 50. AN	112.N 110.N 28.0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH1)	160, N	126'N	38,0N
	(TDOH2)	156, N	124'N	38,0N
	(TDOH3)	144, N	122'N	34,0N
	(TPDH)	142, N	116'N	34,0N
	(TRC)	360, N	288'N	128.N
	(TWC)	248, N	256'N	128.N
IIL	ITH	VICI	AICS	
A0 -1,70NA	1.80NA	3.13 V	93,11 V	
A1 -1,40NA	1.80NA	3.14 V	93,14 V	
A2 +1,50NA	1.40NA	3.16 V	93,18 V	
A3 +1,80NA	2.00NA	3.14 V	93,17 V	
A4 =1,40NA	1,90NA	3,16 V	=3.15 V	PRODUCTORIL FITT OF THE
A5 =1,80NA	1,70NA	3,12 V	=3.11 V	
A6 =1,90NA	1,70NA	3,12 V	=3.11 V	
A7 =1,80NA	1,30NA	3,13 V	=3.14 V	
CS1 -2.20NA	1.70NA	3.13 V	93,12 V	The state of the s
CS2 -2.10NA	1.70NA	3.16 V	93,15 V	
MWR -2.30NA	1.70NA	3.12 V	93,13 V	
MRD +1.50NA	1.60NA	3.13 V	93,12 V	
DIØ =1.90NA	1.80NA	3.17 V	-3,16 V	
DI1 =2.00NA	1.50NA	3.16 V	-3,09 V	
DI2 =2.00NA	2.00NA	3.16 V	-3,15 V	
DI3 =1.80NA	1.90NA	3.15 V	-3,12 V	

RCA	CDP18225D	256 X 4 CMOS	STATIC RAM	31 AUG 78 T	EMP:	25 C	SN:	19
					PAGE	2 OF	10	
	000	001	500	003				
VOL1 VOH1 VOH2	125.MV 120.MV 4.84 V 9.77 V	125,MV 130,MV 4,84 V 9,78 V	135,MV 145,MV 4.84 V 9.77 V	130, MV 140, MV 4, 84 V 9, 78 V				
ION1 IDN2 IDP1 IDP2	6.00MA 15.4MA -2.40MA -5.45MA	5.90MA 14.6MA -2.41MA -5.52MA	5.60MA AMS.21 AMS.24 AMS.24	5,65MA 13,6MA -2,42MA -5,58MA				
1021 1022 1023 1024	20.8NA 16,7NA 18,9NA 22.0NA	16.4NA 18.9NA 17.7NA 14.9NA	22,3NA 18,7NA 18,6NA 22.4NA	15.6NA 18.3NA 19.1NA 16.3NA				
1025 1026 1027 1028	15.2NA 15.4NA 15.6NA 15.1NA	21.0NA 21.6NA 21.1NA 21.1NA	17,3NA 17,0NA 16,9NA 17,1NA	21.5NA 20.7NA 20,8NA 20,3NA				
ILDP	-5,00UA							
IL1 IL2 IL3 IL4	=5.00UA =5.00UA =35.0UA =20.0UA							

RCA CDP1822SD 256 X 4	CMOS STATIC RAM 31 AUG	78 TEMP: +20 C SN:
		PAGE 3 OF 10
PASSED GALPAT (WIDE LI PASSED GALPAT (TIGHT LI FAILFD GALPAT (TIGHT LI		8 DIAG = 57 PTN: 010
PASSED DATA RETENTION TE	ST	
	VCC = 4.5V	5.0V 10.0V
ADDRESS ACCESS TIME NATA SETUP TIME DATA HOLD TIME	(TAA) 455.N (TDS) 28.0N (TDH) 10.0N	335'N 95'ØN 27.ØN 8.ØØN 10.ØN 10.ØN
ADDRESS SETUP TIME ADDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WINTH	(TAS1) 18'.0N (TAS2) 250.N (TAH) =18,0N (TWP) 78.0N	14.0N 4.00N 182.N 56.0N -16.0N -4.00N 70.0N 36.0N
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLO TIME CS2 HOLD TIME	(TCSS1) 294.N (TCSS2) 290.N (TCSH1) 36.0N (TCSH2) 40.0N	164.N 70.0N 148.N 68.0N 32.0N 22.0N 34.0N 22.0N
OUTPU? ACTIVE FROM CS1 OUTPUT ACTIVE FROM CS2 OUTPUT ACTIVE FROM MRD	(TDOA1) 414.N (TDOA2) 412.N (TDOA3) 52.0N	312,N 104.N 312,N 102.N 46.0N 26.0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH1) 152.N (TDOH2) 148.N (TOOH3) 142.N (TPOH) 140.N (TRC) 352.N (TWC) 272.N	118,N 34,0N 116,N 34,0N 118,N 30,0N 114,N 32,0N 272,N 120.N 200.N 112.N
IIL IIH	VIC1 V	ics

	IIL.	IIH	VICI	AIUS
AØ	-200.PA	300.PA	3.22 V	-3,20 V
A1	-300.PA	300.PA	3.24 V	-3,24 V
A2	-300.PA	300.PA	3.25 V	-3,28 V
A3	-400.PA	400.PA	3.24 V	-3,26 V
A4	#300.PA	300,PA	3.26 V	₹3,25 V
A5	#400.PA	300,PA	3.21 V	₹3,20 V
A6	#500.PA	400,PA	3,21 V	₹3,20 V
A7	#400.PA	200,PA	3.22 V	₹3,23 V
CS1 CS2 MWR MKD	~500.PA ~500.PA ~500.PA ~300.PA	300.PA 300.PA 300.PA 300.PA	3.22 V 3.26 V 3.22 V	-7,21 V -3,24 V -3,22 V
010	-400.PA	300.PA	3.27 V	-3,25 V
011	-600.PA	300.PA	3.26 V	-3,18 V
012	-400.PA	700.PA	3.26 V	-3,24 V
013	-400.PA	400.PA	3.25 V	-3,21 V

RCA	CDP1822SD	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP	-20 C	SN	19
	•				PAGE	4 OF	10	
	noø	100	500	003				
VOL1	110.MV	115. MV	120.MV	115, MV				
AOLS	105.MV	115 MV	125.MV	150 MV				
VOH1	4.86 V	4,86 V 9,81 V	4.86 V	4,86 V 9,81 V				
V0H2	9.81 V	9,81 V	9.80 V	9,81 V				
IDN1	6.65MA	6.50MA	6" 20MA	6125MA				
IDNS	17.5MA	16.7MA	15.2MA	15,5MA				
IDP1	-2,83MA	-2,85MA	-2.84MA	-2,86MA				
IDP2	#6.41MA	-6.52MA	=6.37MA	≖6€58MA				
IOZ1	4.30NA	3,50NA	4.30NA	2,30NA				
IOZZ	1.00NA	7.00NA	700.PA	5,90NA				
1023	7,80NA	500,PA	6,10NA	1.20NA				
1024	6,30NA	400 PA	6.30NA	300.PA			•	
1075	1.00NA	6,40NA	AQA.PA	7,20NA				
IOZ6	1,40NA	6,20NA	=100 _* PA	6,70NA				
IUZ7	1,30NA	5,80NA	600.PA	6,70NA				
1078	1,90NA	5.60NA	SØM.PA	6 40NA				
ILDP	-5.00UA							
	-							
ILi	#5.ØØUΛ							
īrz	-5 ,00UA							
IL3	=25,ØUA							
XL4	⇒15,0UA							

RCA CDP1822SD 256	X 4 CMOS ST	ATIC RAM 31	AUG 78 TEMP:	+55 C SN1
			PAGE	5 OF 10
PASSED GALPAT (TIGH	T LIMITS) V	CC=10V CC=10V CC=5V ADD	= 8 DTAG #	57 PIN: 010
PASSED DATA RETENTION	N TEST			
	VC	C = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA) (TDS) (TDH)	505.N 32.0N 8.00N	350,N 26,AN 8,AMN	90 , 0N 8
ADDRESS SETUP TIME ADDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WIDTH	(TAS1) (TAS2) (TAH) (TWP)	16.0N 284.N =20,0N 84.0N	12.9N 196.N -16.AN 70.AN	4.00N 32.0N -2.00N 34.0N
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS1) (TCSS2) (TCSH1) (TCSH2)	334.N 334.N 44.BN 46.BN	176'N 176'N 38'N 38'NN	66, AN 62, AN 22, AN 28, AN
OUTPUT ACTIVE FROM COUTPUT ACTIVE FROM COUTPUT ACTIVE FROM ME	(SAOOT) SE	1.00K 1.00K 50.0N	326', N 326', N 42 , NN	107.N 98,0N 24.0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH1) (TDOH2) (TDOH3) (TPDH) (TRC) (TWC)	146 N 142 N 140 N 140 N 360 N	112, N 110, N 118, N 114, N 272, N 192, N	32,0N 32,0N 30,0N 30,0N 112.N 104.N
IIL	IIH	VIC1	VICP	
A0 = 100.PA A1 = 100.PA A2 = 100.PA A3 = 100.PA	100.PA 100.PA 100.PA 100.PA	3.32 V 3.34 V 3.35 V 3.34 V	-3,34 V -3,38 V -3,36 V	\$400 x
A4 = 100.PA A5 = 100.PA A6 = 100.PA A7 = 100.PA	100.PA 100.PA 100.PA 100.PA	3.36 V 3.31 V 3.30 V 3.31 V	-3,35 V -3,29 V -3,30 V -3,34 V	RODUCIBILITY OF THE
CS1 =100.PA CS2 =100.PA MWR =100.PA MRD =100.PA	100.PA 100.PA 100.PA 100.PA	3.32 V 3.36 V 3.32 V 3.34 V	=3,30 V =3,34 V =3,32 V =3.30 V	. 40°46
DIØ =100.PA DI1 =200.PA DI2 =100.PA DI3 =100.PA	100.PA 100.PA 300.PA 100.PA	3.38 V 3.36 V 3.36 V 3.36 V	+3,35 V +3,28 V +3,34 V +3,30 V	

RCA	CDP1822SD	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP	*55 C S	N: 19
					PAGE	6 OF 10	
	DOØ	001	002	003			
VOH 2 VOH 1 VOH 1	105.MV 100.MV 4.88 V 9.83 V	105.MV 100.MV 4.88 V 9.84 V	110.MV 115.MV 4.88 V 9.84 V	110, MV 110, MV 4, BR V 9, 84 V			
IDN1 ION1 IOP1 IOP2	7,15MA 19,3MA =3,21MA =7,38MA	7.65MA 18.3MA -3.29MA -7.52MA	6_70MA 16_8MA #3_26MA #7_31MA	6.75MA 17.2MA 43.29MA 43.54MA			
1021 1022 1023 1024	4.40NA *100.PA 4.00NA 5.30NA	-500.PA 3.20NA -100.PA -1.90NA	4.00NA =100.PA 3.00NA 5.40NA	-900 PA 2.90NA 800 PA -1.80NA			
1075 1076 1077 1078	-1.30NA -1.30NA -1.10NA -1.10NA	5,40NA 5,00NA 5,00NA 4,60NA	-2.00NA -1.90NA -2.00NA -1.80NA	5,50NA 5,60NA 5,30NA 5,30NA			
ILOP	-5.00UA						
IL1 IL2 IL3 IL4	-5.00UA -5.00UA -25.0UA -15.0UA						

		The second second second second second		and a second distribution of the control of the con
RCA CDP1822SD 256 X 4	CMOS STATI	C RAM 31	AUG 78 TEMPÍ	85 C SN:
			PAGE	7 OF 10
PASSED GALPAT (WIDE LI PASSED GALPAT (TIGHT LI	MITS) VCC=	••		·
PASSED GALPAT (TIGHT LI		•		
PASSED DATA RETENTION TE	ST			
	VCC =	4,5V	5'.0v	10.0V
ADDRESS ACCESS TIME	(TAA)	375.N	300'N	115.N
DATA SETUP TIME DATA HOLD TIME	(TDS) (TDH)	34,0N 14.0N	22.0N 14.0N	10,0N
ADDRESS SETUP TIME	(TAS1)	B. OON	8. 0 M N	6.00N
ADDRESS SETUP TIME	(TAS2)	218.N	176 N	64.0N
ADDRESS HOLD TIME	(TAH)	≈20°0N	-16. ØN	-4.00N
WRITE PULSE WINTH	(TWP)	86.ØN	76.0N	44.0N
CS1 SETUP TIME	(TCSS1)	SQQ.N	162, N	82 ON
CS2 SETUP TIME	(TCSS2)	196 N	158 N	80,0N
CS1 HOLD TIME	(TCSH1)	50,0N	46,0N	28, ØN
CS2 HOLD TIME	(TCSH2)	54.0N	48 mn	28, ØN
OUTPUT ACTIVE FROM CS1	(TDOA1)	362.N	298' N 296' N	122.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	369.N	296.N	120.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	60.0N	54.0N	30.0N
OUTPUT HOLD FROM CS1	(TDOH1)	164.N	132, N	44 ON
OUTPUT HOLD FROM CSS	(TDOH2)	160.N	130,N	44,0N 36,0N
OUTPUT HOLD FROM MRD	(TDOH3)	146,N	130, N 122, N 118, N	36,0N
OUTPUT HOLD FROM MWR	(TPDH)	144 N	118,N	38,0N
READ CYCLF TIME WRITE CYCLF TIME	(TRC) (TWC)	360.N 256.N	296,N 232.N	128 N
ever at 3 to the 3 to \$100.	(184)	630.N	# 3 € * (A	136.N

	TIL	IIH	VIC1	VTCP
AØ	#19.7NA	20.7NA	3.06 V	-3,03 V
Ai	#18,6NA	20.2NA	3.08 V	-3.08 V
A 2	⇔18,8NA	18.8NA	3.09 V	-3,12 V
A3	#19.8NA	AN8.05	3.08 V	-3,11 V
A 4	-18.4NA	20.1NA	3.10 V	-3,09 V
A5	-20,4NA	20.6NA	3.04 V	-3,04 V
A6	#21,0NA	20.5NA	3.04 V	-3,04 V
A7	#20.5NA	18.5NA	3.05 V	=3.08 V
CSI	=21,7NA	20.3NA	3.05 V	-3-04 V
CS2	-20,9NA	20.2NA	3.09 V	=3.10 V
MWR	-21,6NA	19.5NA	3.04 V	-3,06 V
MRD	-19.2NA	19.1NA	3.05 V	#3.05 V
DIØ	m19,4NA	20.6NA	3.11 V	-3,09 V
DII	+20,4NA	19.3NA	3.09 V	-3,02 V
SIO	+20.4NA	20,2NA	3.10 V	#3,09 V
D13	-19,4NA	ANE.NS	3.09 V	-3.05 V

RCA	CDF18225D	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP:	85 C S
					PAGE	8 OF 10
	DOØ	001	poa	003		
VOLI	145.MV	145, MV	155.MV	150, MV		
VOLE	145.MV	155 MV	170 MV	165,MV		
VOHS	4.80 V	4.80 V	4.80 V	4 81 V		
ADHS	9.72 V	9.73 V	9.72 V	4,81 V 9,73 V		
INNI	5.25MA	5.10MA	4.85MA	4, 90MA		
IDNS	13.2MA	12.4MA	11.3MA	11.6MA		
IDP1	-2.00MA	-2,05MA	-2,00MA	-2,03MA		
1Db5	₩4 _# 57MA	-4.64MA	#4.51MA	=4.68MA		
TOZi	167.NA	160,NA	172 NA	174, NA		
Ioza	157.NA	161,NA	170.NA	167,NA		
1023	161 NA	156,NA	169,NA	171, NA		
1074	152.NA	160.NA	172.NA	167 NA		•
1025	160.NA	163.NA	173.NA	174, NA		
1026	161.NA	156,NA	184 NA	164, NA		
1027	167.NA	153,NA	178.NA	175,NA		
IOZ8	158.NA	163.NA	174 NA	170.NA		
ILDP	4.2004					
ILi	-20,0UA					
112	-25.0UA					
ĪĽ3	-45,0UA					
IL4	-35.0UA					
v №	THE RESERVE					

SNE

PASSED GALPAT (WIDE LIMITS) VCC=10V PASSED GALPAT (TIGHT LIMITS) VCC=10V PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

d.

	vcc	= 4.5V	5.0v	10.0v
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA) (COS) (HOT)	365 N 24 ØN 16. ØN	300'N 22.0N 16.0N	125.N 10,0N 14.0N
ADDRESS SETUP TIME ADDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WIDTH	(TAS1) (TAS2) (TAH) (TWP)	6.00N 214.N 418.0N 92.0N	6.00N 174.N -16.0N 8P.0N	6.00N 72.0N -6.00N 46.0N
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS1) (TCSS2) (TCSH1) (TCSH2)	200 N 192 N 54 20 58 00	174°N 168°N 48°0N 52°0N	92,0N 88,0N 30,0N 30,0N
OUTPUT ACTIVE FROM CS: OUTPUT ACTIVE FROM CS: OUTPUT ACTIVE FROM MR	(SAOGT) S	368.N 364.N 64.0N	306 N 304 N 56 ON	130 N 128 N 34 ON
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH1) (TDOH2) (TDOH3) (TPOH) (TRC) (TWC)	166.N 162.N 144.N 146.N 360.N 264.N	136, N 132, N 120, N 120, N 304, N 240, N	48,0N 50,0N 38,0N 38,0N 136,N
IIL	IIH	VIC1	VICP	
A1 =109,NA 1 A2 =108,NA 1	111,NA 109.NA 105,NA 108.NA	3.02 V 3.03 V 3.05 V 3.94 V	-2,99 V -3,03 V -3,09 V -3,06 V	
A5 +114 NA 1	106 NA 110 NA 109 NA 105 NA	3.06 V 3,00 V 3,00 V 3,01 V	73/05 V 43/00 V #3/00 V #3/04 V	
CS2 =114.NA 1	109.NA 111.NA 106.NA 105.NA	3.01 V 3.05 V 3.00 V 3.01 V	-3,00 V -3,06 V -3,02 V -3,01 V	
DI2 =100.NA 1	109,NA 108,NA 109,NA 106.NA	3,06 V 3,05 V 3,05 V 3,04 V	=3,05 V =2,98 V =3,05 V =3.01 V	

RÇA	CDP182250	256 X 4	CMOS	STATIC R	AM 31	AUG	78	TEMP	125 C	\$N:	19
								PAGE	ia ne	10	

	DOØ	001	500	003
VOL1 VOH1 VOH2	160.MV 160.MV 4.78 V 9.69 V	160.MV 170.MV 4.78 V 9.70 V	170.MV 190.MV 4.78 V 9.68 V	170, MY 185, MV 4,78 V 9,70 V
IDN1 IDN2 IDP1 IDP2	4.70MA 11.7MA -1.82MA -4.11MA	4.60MA 11.2MA -1.83MA -4.15MA	4.35MA 10.0MA -1.81MA -4.05MA	4.45MA 10.4MA -1.85MA -4.22MA
T0Z1 T0Z2 T0Z3 T0Z4	623.NA 610.NA 605.NA 602.NA	561,NA 555.NA 549,NA 552.NA	687,NA 674,NA 675,NA 666,NA	AN,256 AN,256 AN,856
1025 1026 1027 1028	616,NA 606,NA 606,NA 611,NA	566.NA 578,NA 561,NA 565.NA	693.NA 684.NA 692.NA 683.NA	647,NA 635,NA 628,NA 641.NA
ILOP	PO.OUA			
ILI ILZ IL3 IL4	-85.0UA -105.UA -115.UA -85.0UA			

PAGE 1 OF 10

	r Limits) v	CC=10V CC=10V CC=5V	REPRODUCIBI ORIGINAL PA	LITY OF THE GE IS POOR
PASSED DATA RETENTION	N TEST			
	VC	C = 4,5V	5.0V	iø,øv
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA) (TDS) (TDH)	16,0N 16,0N 18,0N	190'.N 14.0N 10.0N	75,0N 6.00N 10.0N
ADDRESS SETUP TIME ADDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WINTH	(TAS1) (SAS) (TAH) (TWF)	8.00 118. -16.0 -16.0 -16.0	8'.00N 96.0N -17.0N 48.0N	4.00n 40.0n -2.00n 30.0n
CS: SETUP TIME C32 SETUP TIME CS: HOLD TIME CS: HOLD TIME	(TCSS1) (TCSS2) (TCSH1) (TCSH2)	126.N 32,0N	112,N 108,N 30,0N 30,0N	58,0N 56,0N 20,0N 18,0N
OUTPUT ACTIVE FROM COUTPUT ACTIVE FROM MO	(SADOT) Sa	N.858	190, N 188. N 40. ØN	86,0N 84,0N 24,0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH1) (TDOH2) (TDOH3) (TPOH) (TRC) (TWC)	136 N	108, N 108, N 114, N 110, N 200, N 144, N	30,00 30,00 30,00 36,00 96,00 96,00
IIL	IIH	VICI	VICE	
A0 =1.90NA A1 =1.90NA A2 =1.80NA A3 =1.90NA	1.60NA 1.90NA 1.90NA 2.00NA	3.13 V 3.15 V 3.18 V 3.17 V	+3,10 V +3,19 V +3,19 V	
A4 =1.90NA A5 =1.70NA A6 =1.80NA A7 =2.00NA	2,10NA 1,80NA 1,70NA 2,20NA	3.19 V 3.11 V 3.10 V 3.11 V	-3/22 V -3/17 V -3/16 V -3/14 V	
CS1 -1,90NA CS2 -1,90NA MWR -2,50NA MRD -1,80NA	1.60NA 1.80NA 1.90NA 1.90NA	3.19 V 3.24 V 3.11 V 3.16 V	#3/19 V #3/26 V #3/13 V #3/17 V	
DIØ #2.20NA DII #1.80NA DI2 #1.60NA DI3 #1.70NA	2,00NA 2,00NA 2,00NA	3.26 V 3.22 V 3.28 V 3.24 V	-3,19 V -3,18 V -3,23 V -3,23 V	
		B-191		

RÇA	CDP182250	256 X 4 CHOS	STATIC RAM	31 AUG 78	TEMP:	25 C SN:	20
					PAGE	2 OF 10	
	NOO	D01	nos	003			
AOHS AOHI AOFI	100.MV 115.MV 4.85 V 9.76 V	105,MV 125,MV 4,85 V 9,76 V	115,MV 140,MV 4,84 V 9,76 V	115,MV 140,MV 4,84 V 9,75 V			
ION1 IOP1 IOP2	7.30MA 16.6MA -2.61MA -5.19MA	6,95MA 15,4MA -2,63MA -5,25MA	6.45MA 13.6MA -2.53MA -5.05MA	6.50MA 13.8MA -2.55MA -5.00MA			
1021 1022 1023 1024	10,0NA 12,2NA 12,4NA 9,70NA	14.4NA 11.3NA 10.4NA 13.3NA	7,40NA 9,60NA 11,6NA 8,20NA	15.9NA 18.1NA 10.0NA 13.2NA			
1025 1026 1027 1028	14,8NA 14,6NA 14,6NA 14,4NA	8,500A 8,900A 8,600A 8,800A	11,3NA 11,6NA 11,3NA 11,6NA	10.9NA 10.7NA 10.7NA 10.6NA			
ILDP	-10.0UA						
IL1 IL2 IL3 IL4	-5,00UA -5,00UA -25,0UA -20,0UA						

RCA	CDP1822SD	256 X 4	CMOS STATIC RAM	31 AUG 78	TEMP:	-20 C	SN:	20
					PAGE	3 OF 1	Ø	

PASSED GALPAT (WIDE LIMITS) VCC=10V PASSED GALPAT (TIGHT LIMITS) VCC=10V PASSED GALPAT (TIGHT LIMITS) VCC=5V

	- ·			
	VCC	= 4.5V	5 . 0v	10.0V
ADDRESS ACCESS TIME	(TAA)	245.N	185 N	70.0N
DATA SETUP TIME	(TDS)	18.ØN	14.7N	
DATA HOLD TIME	(TDH)			6.00N
WHIR HOWN TIME	CIDNI	8.00N	8.00N	10.0N
ADDRESS SETUP TIME	(TAS1)	12,0N	8.ตกท	4 . ØØN
ADDRESS SETUP TIME	(TASE)	128.N	96.00	36.0N
ADDRESS HOLD TIME	(TAH)	-16, ØN	-12.0N	-2.00N
WRITE PULSE WINTH	(TWP)	60 0N	46.AN	58. QM
West was a second secon	•	19 19 II	404	_ G _ G
CS1 SETUP TIME	(TCSS1)	126.N	108 N	54,0N
CS2 SETUP TIME	(TCSS2)	155 N	106.N	รลโดท
CS1 HOLD TIME	(TCSH1)	28, ØN	24.01	18,0N
CS2 HOLD TIME	(TCSH2)	30 ์ ØN	26. MN	16.0N
	,	# 4		10801
OUTPUT ACTIVE FROM CS1	(TDOA1)	242.N	192 N	80,0N
OUTPUT ACTIVE FROM CS2	(TDOAZ)	240.N	190 N	78, ØN
OUTPUT ACTIVE FROM MRD	(TDOA3)	42. ØN	36.0N	22.0N
• •				2 2 2 2 4 2 4 4
OUTPUT HOLD FROM CS1	(TDOH1)	132.N	105 N	30,0N
OUTPUT HOLD FROM CS2	(SHOOT)	130.N	100 N	30.0N
OUTPUT HOLD FROM MRO	(TDOH3)	134.N	112,N	28,00
OUTPUT HOLD FROM MWR	(TPDH)	132.N	108 N	28, ØN
READ CYCLE TIME	(TRC)	216 N	108 N	
WRITE CYCLE TIME	(TWC)	176.N	184,N 144.N	88,0N 88.0N
		F O 14	# m - 4 # 14	00804
IIL IIH		vici	VICA	•
AØ -200,PA 200	-ΡΔ ·	3.20 V	+3,16 V	
	.PA	3.83 V	-3°56 ∧	
	PA	3.24 V	-3,26 V -3,25 V	
	PA	3.24 V	43.25 V	
	a N	Darte A	43.27 V	
A4 #390,PA 300	-PA	3.26 V	-3,28 V	
A5 -300.PA 200	•	3,17 V	- 3,23 ∨	
- · ·	PA	3.16 V	3.22 V	
	PA	3.17 V	-3,20 V	
			704	
CS1 =300.PA 200	"PA	3,26 V	-3,25 V	
CS2 -300.PA 200	.PA	3,30 V	43,32 V	
MWR -500.PA 300	, PA	3.18 V	=3,38 V =3,38 V	
MRD -200.PA 300		3.23 V	-3.23 V	
				
DIØ -300.PA 200		3.33 V	-3,25 V	
0I1 =200.PA 300	≠ ₽A	3.29 V	-3,24 V	
DIS #200.PA 300	PΑ	3.35 V	#3,29 V	
DI3 -200,PA 400	_PA	3.31 V	-3,29 V	

RCA	CDP1822SD	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMPi	#20 C	SNI	20
	•				PAGE	4 OF	10	
	២០២	D01	pos	2003				
00H2 00H1 00H1 VOL1	90,0MV 105,MV 4,87 V 9,79 V	95,0MV 110.MV 4,87 V 9,80 V	105,MV 125,MV 4,87 V 9,78 V	100 MV 125 MV 4 86 V 9 77 V				
IDN1 IDN2 IOP1 IOP2	8.00MA 18.2MA -2.97MA -5.83MA	7'.60MA 16.9MA -2.99MA -5.91MA	7_15MA 15_0MA =2_94MA =5_72MA	7.15MA 15.3MA -2.88MA -5.55MA				
1071 1072 1073 1074	3.00NA 300.PA 7.40NA 5.30NA	4,00NA 7,10NA -100,PA 300,PA	2.90NA =400.PA 6.20NA 5.20NA	2,70NA 6.30NA 400,PA 200.PA				
1025 1076 1027 1028	800.PA 1.10NA 1.00NA 1.30NA	5.70NA 5.80NA 5.40NA 5.50NA	=400.PA =400.PA =300.PA =400.PA	6,50NA 6,20NA 6,40NA 6.20NA				
ILDP	∾5.00UA							
IL1 IL2 IL3 IL4	₩5,00UA ₩5,00UA ₩20,0UA							

PASSED GALPAT (WIDE LIMITS) VCC=10V PASSED GALPAT (TIGHT LIMITS) VCC=10V PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

	,,			
	Acc	= 4.5V	5'.ØV	10.0V
ADDRESS ACCESS TIME	(TAA)	245.N	180'N	65'. ØN
DATA SETUP TIME	(TDS)	20.0N	16. AN	6.00N
DATA HOLD TIME	(TDH)	8,00N	8.00N	8,000
	(15.17	4.500.4	A B Frank	11.00
ADDRESS SETUP TIME	(TAS1)	10.0N	8.00N	4 . Ø Ø N
ADDRESS SETUP TIME	(TAS2)	130 N	96,0N	32. ØN
ADDRESS HOLD TIME	(TAH)		-10.0N	-2.90N
WRITE PULSE WIDTH	(TWP)	-14,0N 52.0N	46.AN	56.0N
MUTTE OFSE WINTO	(1111)	35 9 St	sh Cl ^{te} A⊣A	40 P 41 A
CS1 SETUP TIME	(TCSS1)	122 M	104 N	50,0N
CS2 SETUP TIME	(TCSS2)	122.N	1. (2) (4) (4) (4) (4) (4) (4) (4) (4) (4) (4	
·		120.N	102.N	48,0N
	(TCSH1)	32,ØN	54 W	18, ØN
CS2 HOLD TIME	(TCSH2)	32.0N	96.WN	14 . UN
AUTOUT ACTIVE FOOR OF		****	400' 11	94 (90
OUTPUT ACTIVE FROM CS		258,N	192'N	76, ØN
OUTPUT ACTIVE FROM CS	•	254 N	184.N	74, ØN
OUTPUT ACTIVE FROM MR	D (TDGA3)	38,0N	34.0N	20.0N
A1196119 11015 FEB.		i		m f
OUTPUT HOLD FROM CS1	(TDOH1)	128 N	98.0N	30,0N
OUTPUT HOLD FROM CS2	(SHOUT)	126.N	96.PN	32,0N
OUTPUT HOLD FROM MRD	(TDOH3)	134.N	112,N	26,0N
OUTPUT HOLD FROM MWR	(TPOH)	130.N	108; N	28,0N
READ CYCLE TIME	(TRC)	208.N	176,N	96 DN
WRITE CYCLE TIME	(TWC)	152.N	144.N	80.0N
TIL	IIH	VIC1	AICS	
A0 +100.PA	0 00 A	3.26 V	-3,22 V	
	100.PA	3,28 V	73,32 V	
	100,PA	3,30 V		
	100.PA	3.29 V	93,31 V -3.31 V	
A3 SINUERA	TAM * L M	7°52 A	-3.31 V	
A4 -100.PA	an'na	2 24 H	- 7' 7 t 11	
· · · · · · · · · · · · · · · · · · ·	100,PA	3.31 V	-3,34 V	
	100.PA	3.82 V	-3,29 V	
A6 0,00 A	100,PA	3,22 V 3,23 V	-3,28 V	
A7 -100.PA	100.PA	3.23 V	-3,26 V	
70 4				
CS1 -100.PA	100, PA	3,32 V	-3,31 V	
CS2 -100.PA	100 PA	3,36 V	-3,38 V	
MWR #100,PA :	100,PA	3.25 V	73,38 V 73,25 V	
MRD #100.PA	100.PA	3.29 V	=3.29 V	
010 =100.PA (0 00 A	3.38 V		
	100,PA	3.35 V	-3,31 V -3,29 V -3,35 V	
	100.PA	3.40 V		
	100.PA	3.37 V	73,37 V 73.35 V	
ORD VENN N	TOURTH	a a a l	₩ ⊅⊕ ₫7 ¥	
		D 105		

RCA CDF1822SD 256 X 4 CMOS STATIC RAM 31 AUG 78 TEMP1 -55 C SN1 20

-	•		•	OF	4 7
	А	GE	_	112	10
	-	IR L.	·	W (1.1

	DOØ	001	002	200
VOL1	85,0MV	90.0MV	95'.ØMV	95.0MV
VOL2	95,0MV	105.MV	115.MV	115.MV
VOH1	4,88 V	4.88 V	4.88 V	4.88 V
VOH2	9,80 V	9.81 V	9.80 V	9.80 V
IDN1	8.65MA	8.30MA	7.75MA	7.75MA
IDN2	19.5MA	18.3MA	16.3MA	16.5MA
IDP1	-3.35MA	-3.39MA	=3.32MA	73,21MA
IDP2	-6.51MA	-6.38MA	=6.34MA	-6.08MA
1021	3.60NA	-100 PA	3.30NA	-700.PA
1022	#400.PA	3 50NA	=400.PA	3.00NA
1023	4.10NA	-400 PA	2.90NA	500.PA
1024	5.00NA	-1 90NA	5.10NA	-1.90NA
1025	-1.50NA	5,20NA	-2.20NA	5,30NA
1026	-1.60NA	5,00NA	-2.20NA	5,40NA
1027	-1.50NA	5,10NA	-2.20NA	5,20NA
1028	-1.60NA	4,90NA	-2.20NA	5,40NA
ILDP	-10.ØUA			
IL1 IL2 IL3 IL4	-5.00UA -5.00UA -15.0UA -20.0UA			

RCA	CDP1822SD	256 X 4	CMOS STATIC	RAM 31	AUG 78	TEMPI	85 C	SN:	50
						n.or	7 65 1	G.	

PASSED	GALPAT	(WIDE	LIMITS)	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS)	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS)	VCC=5V

- Man is the a white with the same	1 1-11			
	vcc	= 4,5V	5.0V	10'.0V
ADDRESS ACCESS TIME	(TAA)	215.N	185.N	80°0N
DATA SETUP TIME	(TDS)	16,0N	14.0N	8.00N
DATA HOLD TIME	(TDH)	12.0N	12.0N	12.0N
SATA NOED (11/2	CIDITY	1 2 2 5 4		14.50
ADDRESS SETUP TIME	(TAS1)	6.00N	6 , 00N	4,00N
ADDRESS SETUP TIME	(TAS2)	112.N	. 92.0N	44.0N
ADDRESS HOLD TIME	(TAH)	-14° ØΝ	#12.0N	-5.60N
WRITE PULSE WINTH	(TWP)	62.ØN	54.0N	34.0N
OC. ONTHE BANK	4M00043	470 11	4 4 4 F 5.	d m f mus
CS1 SETUP TIME	(TCSS1)	132,N	116 N	45, QN
CS2 SETUP TIME	(TCSS2)	130.N	114.N	60 - 0N
CS1 HOLD TIME	(TCSH1)	38,0N	35.WN	ECADIN
CS2 HOLD TIME	(TCSH2)	38. ØN	34.9N	22.0N
OUTDIT LOTTUE COOK ACT	(700443	222 At	4 Marsh Si	อก็อง
OUTPUT ACTIVE FROM CS1	(TDOA1)	855 N	190,N	94, ØN
OUTPUT ACTIVE FROM CS2	(SABOT)	218.N	188.N	92,0N
DUTPUT ACTIVE FROM MRD	(TDOA3)	46 " BN	42.0N	56.QN
OUTPUT HOLD FROM CS1	(TOOH1)	140.N	110,N	32, ØN
OUTPUT HOLD FROM CS2	(SHOOT)	138 N	MR N	34 0N
OUTPUT HOLD FROM MRD	(TDOH3)	138.N	108, N	34,0N 30,0N
			116.N	ייש אַ שַׁרָּב
CUTPUT HOLD FROM MWR	(TPOH)	134 N	110,N 208,N	30.0N
READ CYCLE TIME	(TRC)	240.N	N BNS	104.N
WRITE CYCLE TIME	(TWC)	176.N	160.N	104.N
iir i.	Tн	VICI	VICE	
AØ #27,6NA 20	6.6NA	3,11 V	-3,07 V	
	8.1NA	3,13 V	-3,16 V	
	B.1NA	3.15 V	-3,17 V	
	B ZNA	3.14 V	-3.16 V	
	-			
A4 =27.7NA 28	B.4NA	3.16 V	-3,19 V	
A5 #26,8NA 20	6.3NA	3.08 V	-3,14 V	
	7.3NA	3.07 V	-3,13 V	
A7 -28.0NA 29	9.4NA	3.08 V	#3.11 V	
	•	-	· • · · · · · · · · · · · · · · · · · ·	
	7.2NA	3.17 V	-3,16 V	
	9.5NA	3.21 V	-3,24 V	
	7.7NA	3,48 V	v 3 , 11 V	
MRD =28,0NA 2	B _a 5NA	3.14 V	-3.14 V	
DIØ #28.5NA 2'	7.6NA	3 3/L V	-3,17 V	
		3.24 V	٧ ١ م ترم الا تاكام ت	
	7.9NA	3.20 V	-3,15 V	
	9.1NA	3.85 V	-3,20 V	
DI3 #27.0NA 28	8,8NA	3.22 V	-3.20 V	

RCA	CDP1822SD	256 X 4 CMOS	STATIC RAM	31 AUG 78 1	TEMP:	85 C	SN:	20
					PAGE	8 OF	10	
	000	100	500	003				
VOL1 VOL2 VOH1	115.MV 130.MV 4.82 V 9.72 V	120,MV 140,MV 4,82 V 9,73 V	130.MV 160.MV 4.82 V 9.72 V	130 MV 160 MV 4,82 V 9,72 V				
ION1 ION2 IOP1 IOP2	6,45MA 14,7MA =2,24MA =4,53MA	6.10MA 13.5MA -2.26MA -4.61MA	5,70MA 11,9MA =2,21MA =4,42MA	5,75MA 12,2MA 22,21MA 44,42MA				
1021 1022 1023 1024	4.30NA 1.10NA -1.40NA -2.30NA	-15,0NA -20,4NA -27,7NA -24,2NA	-25,9NA -27,1NA -25,3NA -27.8NA	-6,70NA -9,60NA -16,7NA -13,6NA				
IUZ5 IOZ6 IOZ7 IOZ8	-100 PA 1 20 NA -1 70 NA 1 00 NA	-27.6NA -28.4NA -28.8NA -29.1NA	-27,0NA -27,6NA -26,8NA -26,6NA	#17,2NA #16,7NA #16,8NA #16,7NA				
ILDP	7.46UA							

=35,0UA =40,0UA =50,0UA =45,0UA

IL1 IL2 IL3 IL4

### PASSED GALPAT (#IDE LIMITS) VCC#16V PASSED GALPAT (TIGHT LIMITS) VCC#16V PASSED G				PÂGE	9 OF 11
VCC = 4.5V 5.0V 10.0V	PASSED GALPAT C	TIGHT LIMITS) \ TIGHT LIMITS) \	/CCH10V	REPRODUCIBILIT ORIGINAL PAGE	Y OF THE IS POOR
ADDRESS ACCESS TIME (TAA) 225.N 199.N 98.8N OATA SETUP TIME (TDS) 16.0N 14.0N 8.90N ADDRESS SETUP TIME (TAB1) 4.00N 4.00N 75.0N ADDRESS SETUP TIME (TAB2) 114.N 96.0N 75.0N ADDRESS MOLD TIME (TAB2) 114.N 96.0N 75.0N 86.0N 8	hand and the section of the			. t	t .
DATA SETUP TIME (TDS) 16.0N 12.0N 12		۸t	C = 4,5V	5. 0V	10.0V
ADDRESS SETUP TIME (TASE) 114 N 96.0N 50.0N 22.0N WRITE PULSE WIDTH (TWP) 64.0N 58.0N 36.0N DATA SETUP TIME	(TDS)	225.N 16.0N 12.0N	14,0N	8.ggN	
CS1 HOLD TIME (TCSH1) 38,0N 34,0N 22,0N 22	ADDRESS SETUP TI ADDRESS HOLD TIM	ME (TAS2) E (TAH)	114 N =14 p D N	96.0N #12.0N	50.0N
OUTPUT ACTIVE FROM CS2 (TDOAS) 332.N 200.N 309.N 309.N 309.N 309.N 34.0N	CS2 SETUP TIME CS1 HOLD TIME	(TCSS2) (TCSH1)	136.N 38.0N	132.N 34,0N	55' QN
OUTPUT HOLD FROM MWR (TPOH) 134.N 112.N 32.0N READ CYCLE TIME (TRC) 248.N 216.N 120.N 120.N WRITE CYCLE TIME (TWC) 184.N 176.N 118.N 118.N 118.N 176.N 118.N	OUTPUT ACTIVE FR	OM CS2 (TDOAR)	N.SES	Sõ@*N	180.N 28.DN
A0 =165.NA 157.NA 3.12 V #3.15 V A3 =165.NA 163.NA 3.14 V #3.15 V A3 =166.NA 163.NA 3.15 V #3.15 V A4 =165.NA 165.NA 3.16 V #3.15 V A5 =162.NA 156.NA 3.06 V #3.13 V A6 =165.NA 160.NA 3.06 V #3.13 V A7 =165.NA 167.NA 3.06 V #3.10 V CS1 =175.NA 167.NA 3.20 V #3.23 V MWR =168.NA 161.NA 3.06 V #3.10 V	OUTPUT HOLD FROM OUTPUT HOLD FROM READ CYCLE TIME	CSŽ (TDOHŽ) MRD (TDOHŽ) MWR (TPOH) (TRC)	138,N 138,N 134,N 248,N	110, N 116, N 112, N 216, N	150"M 150"M
A3	IIL	IIH	VICI	AICS	
A4 #165.NA 163,NA 3,15 V #3,18 V A5 #162,NA 156,NA 3,06 V #3,13 V A6 #165.NA 160,NA 3,05 V #3,12 V A7 #165.NA 167.NA 3,06 V #3,14 V #3,14 V #3,14 V #3,14 V #3,15 V #3,15 V #3,15 V #3,15 V #3,16 V #3,15 V #3,16 V #3,16 V #3,16 V #3,16 V #3,16 V	A1 =163,NA A2 =168,NA	163,NA 163,NA	⊃bîn A	#3,05 V #3,15 V #3,15 V	
CS2 ⇒171,NA 171,NA 3,20 V →3,23 V MWR →168,NA 161,NA 3,06 V →3,10 V	A5 0162.NA A6 0166.NA	156,NA 160,NA	3,06 V 3,05 V	#3,18 ∀ #3,13 V	
	CS2 =171.NA MWR =168.NA	171,NA 161,NA	3,20 V 3,06 V	#3,14 V #3,2% V #3,10 V	

. 4

6.2

- Y 41/2

2472 2

DIØ

DII 015

713

#166.NA

-163.NA

53,15 V 53,14 V 53,19 V 53,19 V 161 NA 159 NA 3.23 V -162.NA 3,18 V #163.NA 168,NA 3,24 V

166.NA

3.21 V

RÇA	CDP1822SD	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP	125 C SN:
					PAGE	10 OF 10
	DOD	001	son	200		
AOH 5 AOH 5 AOH 5 AOH 1	125.MV 140.MV 4.81 V 9.69 V	135 MV 155 MV 4 80 V 9 69 V	145 MV 175 MV 4,80 V 9,69 V	145.MV 175.MV 4.80 V 9.69 V		
1001 1901 Squi	5.85MA 13.5MA -2.05MA -4.16MA	5.55MA 12.4MA -2.07MA -4.20MA	5.15MA 10.8MA -2.00MA -4.03MA	5,20MA 11.2MA -2,04MA -4,10MA		
1021 1022 1023 1024	=366,NA =378,NA =388,NA =381,NA	-493,NA -506,NA -506,NA -515,NA	=496 NA =499 NA =506 NA =503 NA	=438, NA =445, NA =445, NA =453, NA		
1075 1076 1077 1078	-380.NA -380.NA -385.NA -388.NA	-507,NA -523.NA -517.NA -514.NA	=506,NA =505.NA =518,NA =509,NA	7457 NA 7452 NA 7445 NA 7454 NA		

RCA	CDP18228D	256	X d	4	CHOS	STATEC	RAM	31	AUG	78	TEMP	25	C	SN:	21
											PAGE	Ì	OF	10	

PASSED GALPAT (WIDE LIMITS) VCC*10V PASSED GALPAT (TIGHT LIMITS) VCC*10V PASSED GALPAT (TIGHT LIMITS) VCC*5V

. 40000	PATH INDICATED	, 1001			
		vcc	# 4.5V	5.0v	10,0V
DATA S	S ACCESS TIME SETUP TIME HOLD TIME	(TAA) (TDS) (TDH)	285 N 24,0N 14.0N	235', N 20', ON 14. ON	95.0N 8.00N 12.0N
ADDRES	SS SETUP TIME SS SETUP TIME SS HOLD TIME PULSE WINTH	(TAS1) (TAS2) (TAH) (THT)	18 0N 136 N -18,0N 78,0N	14.0N 116.N =16.0N 68.0N	58.00 58.00 4.000 4.000
CS2 S	BETUP TIME BETUP TIME HOLD TIME HOLD TIME	(TCSS1) (TCSS2) (TCSH1) (TCSH2)	188	160°N 158°N 36°N 36°N	78,0N 78,0N 22,0N 22,0N
OUTPUT	ACTIVE FROM CO ACTIVE FROM CO ACTIVE FROM M	(SADOT) SE	262, N 258, N 58, N	555°N 555°N 554°N	106.N 104.N 30.0N
OUTPUT OUTPUT OUTPUT READ O	HOLD FROM CS1 HOLD FROM CS2 HOLD FROM MWR HOLD FROM MWR YCLE TIME CYCLE TIME	(TDOH1) (TDOH2) (TDOH3) (TPOH) (TRC) (TWC)	160, N 150, N 144, N 142, N 288, N 264, N	128, N 124, N 122, N 118, N 248, N 232, N	40,0N 40,0N 36,0N 128.N 128.N
	IIL	IIH	AICT	VICE	
AØ A1 A2 A3	=1.80NA =1.50NA =1.50NA =2.80NA	1,70NA 1,60NA 1,50NA 1,70NA	3.17 V 3.18 V 3.20 V 3.19 V	93,21 V 93,21 V 93,21 V 93,21 V	
A4 A5 A6 A7	-1.50NA -1.50NA -1.50NA -1.40NA	1,70NA 1,90NA 2,50NA 2.00NA	7,22 V V E1.E V E1.E V E1.E	-3,19 V -3,16 V -3,17 V -3,15 V	
CS1 C32 MWR MRD	#1.50NA #1.90NA #1.70NA #1.50NA	1,50NA 1,80NA 1,40NA 1,60NA	3,16 V 3,18 V 3,13 V 3,14 V	#3,17 V #3,17 V #3,16 V #3,14 V	
DIO DII DIZ DI3	#2.20NA #2.40NA #1.80NA #1.90NA	2,10NA 2,50NA 2,20NA 2.00NA	3.23 V 3.23 V 3.22 V 3.20 V	#3,22 V #3,16 V #3,17 V #3,16 V	

RCA	COP1822SD	256 X 4 CHOS	STATIC RAM	31 AUG 78	TEMP:	25 C	SN:	51
					PAGF	2 OF	10	
	DOA	001	500	200				
AOH 5 AOH 1 AOF 5 AOF 1	120.MV 125.MV 4.83 V 9.76 V	125,MV 135.MV 4,84 V 9.76 V	130.MV 150.HV 4.82 V 9.74 V	130, MV 145. MV 4, 83 V 9, 76 V				
ION1 ION2 IDP1 IDP2	6.15MA 15.4MA -2.30MA -5.13MA	6.00MA 14.3MA ~2.30MA ~5.16MA	5.65MA 12.8MA 92.24MA 94.97MA	5.65MA 13.1MA =2.32MA =5.24MA				
1021 1022 1023 1024	35,8NA 32,7NA 30,0NA 33,5NA	28.7NA 30.1NA 33.4NA 29.7NA	34,7NA 32,6NA 27,9NA 31.0NA	28,5NA 29.3NA 34,1NA 31.3NA				
1025 1026 1027 1028	30.1NA 30.5NA 30.1NA 30.1NA	32.6NA 33.1NA 32.7NA 32.8NA	29,8NA 29,7NA 29,8NA 29,6NA	32,9NA 32,5NA 32,9NA 38,4NA				
ILDP	-20,0UA							
IL1 IL2 IL3 IL4	⇔5.00UA ⇔5.00UA ⇔35.0UA ⇔30.0UA							

	LIMITS)	VCC=10V VCC=10V VCC=5V	REPRODUCIBILITY ORIGINAL RASE I	of the S Poo r
PASSED DATA RETENTION	TEST		•	
	٧	CC = 4,5V	5.0V	10,0V
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	CTAA) CTDS) CTDH)	285.N 28,0N 12.0N	23p'n 23,0n 10,0n	90.0N 8.00N 10.0N
ADDRESS SETUP TIME ADDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WIDTH	C!SAT) (SSAT) (HAT) (GWT)		16.0N 184.N 014.0N 70.0N	6.00N 50.0N 54.00N 36.0N
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSSI (TCSSE (TCSH1 (TCSH2	174.N 136,0N	150'N 150'N 32'0N 34'0N	72,0N 70,0N 22,0N 22,0N
OUTPUT ACTIVE FROM CS OUTPUT ACTIVE FROM ME OUTPUT ACTIVE FROM ME	SA (TDOAS	1) 258.N	216'N 214'N 46.0N	98,0N 96,0N 86,0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH1 (TDOH2 (TDOH3 (TPOH) (TRC) (TWC)	148 N 142 N	116, N 116, N 120, N 116, N 224, N 208, N	34,000 34,000 34,000 34,000 120.0 112.0
IIL	11H	VICI	Aics	
A0 +300,PA A1 +200.PA A2 +200.PA A3 +700.PA	300',PA 300,PA 200,PA 200.PA	3,25 V 3,25 V 3,27 V 3,26 V	55,28 V 55,28 V 55,28 V	
A4 =300.PA A5 =400.PA A6 =300.PA A7 =200.PA	300,PA 300,PA 500,PA 400.PA	3.29 V 3.21 V 3.21 V	26 V 25,23 V 25,23 V 25,23 V	
CS1 =300,PA CS2 =400,PA MWR =400,PA MRD =300,PA	300,PA 300,PA 300,PA 400.PA	3.24 V 3,26 V 3,21 V 3,22 V	.3'25 V .3'23 V .3'23 V .5'21 V	
DIO =400 PA DI1 =500 PA DI2 =300 PA DI3 =300 PA	300,PA 400,PA 400,PA 400,PA	3,30 V 3,31 V 3,30 V 3,28 V	-3,29 V -3,24 V -3,25 V	

RCA	CDP1822S0	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP:	≖aø c	sn:
					PAGE	4 OF 10	
	000	001	201	003		·	
AOH5 AOF5 AOF7	105.MV 110.MV 4,86 V 9.80 V	110,MV 115.MV 4,86 V 9.80 V	115.MV 130.MV 4.86 V 9.79 V	115, MV 125, MV 4,86 V 9,80 V			
IDN1 IDN2 IDP1 IDP2	6,90MA 17,5MA +2,69MA +5,97MA	6'.70MA 16.4MA -2,73MA -6.11MA	6,35MA 14.8MA +2,65MA +5,83MA	6.35MA 15.0MA -2.74MA -6.13MA			
1021 1022 1023 1024	2,10NA 4.20NA 5.90NA 2.40NA	8,50NA 5,60NA 2,60NA 6,10NA	1.30NA 2,70NA 6.30NA 2.90NA	8,800A 6,800A A00A 5,900A			
10Z5 10Z6 10Z7 10Z8	6.30NA 6.50NA 6.20NA 6.40NA	3,20NA 3,00NA 3,30NA 3,00NA	5.30NA 5.00NA 5.10NA 4.60NA	4,60NA 4,60NA 4,60NA 4,60NA			
ILDP	-10 <u>.</u> 0U∧						

#5.00UA #5.00UA #25.0UA

IL1 IL2 IL3 IL4

RCA COP1822SO 256 X 4 CMOS STATIC RAM 31 AUG 76 TEMP: W55 C SN: 21

PASSED GALPAT (WIDE LIMITS) VCC#10V PASSED GALPAT (TIGHT LIMITS) VCC#10V PASSED GALPAT (TIGHT LIMITS) VCC#5V

PASSED DATA RETENTION TEST

. HOORD DAIN UPIEMITON IN	Ψ 1			
	VCC	# 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA) (TDS) (TDH)	289.N 32.GN 8.00N	8.00N 8.00N 8.00N	85'. ØN 6. ØØN 1 Ø. ØN
ADDRESS SETUP TIME ADDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WIDTH	(TAS1) (TAS2) (TAH) (TWP)	18.0N 126.N -20.0N -0.0N	14.PN 102.N ~16.QN 60.QN	6. pon 48. dn 4. pon 54. dn
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSSI) (TCSS2) (TCSH1) (TCSH2)	174.N 174.N 42,0N 46.0N	146 N 142 N 36 M 38 M	66,0N 66,0N 22,0N
OUTPUT ACTIVE FROM CS1 OUTPUT ACTIVE FROM MRD	(faody) (saody) (eaody)	260.N 258.N 50.0N	210, N 208. N 44. NN	90,0N 88,0N 26,0N
OUTPUT HOLD FROM C81 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH1) (TDOH2) (TDOH3) (TPOH) (TRO) (TWO)	144 N 140 N 142 N 138 N 248 N 248 N	1 2 6 N 1 9 8 C N 1 1 4 6 C N 2 1 6 C N 2 1 6 C N	12,0N 10,0N 12,0N 120,N 120,N
IIL III	1	VICI	AICS	
A1 0.00 A 100 A2 0.00 A 100	D,PA D,PA D,PA D,PA	3.34 V 3.39 V 3.34 V	.3.29 V .3.36 V .3.36 V	
A5 ~100.PA 100 A6 *100.PA 100	ZPA ZPA ZPA	3,37 V 3,29 V 3,27 V 3,29 V	73,34 V 73,31 V 73,32 V 73,30 V	
CS2 #100,PA 100 MNR #100,PA 100	2	3,32 V 3,35 V 3,30 V 3,30 V	-3,38 V -3,31 V -3,32 V -3,29 V	
011 •200,PA 100 012 •100,PA 100	2.PA 2.PA 2.PA	3,38 V 3,39 V 3,38 V 3,36 V	23,37 V 23,31 V 23,32 V 23,30 V	

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RCA	CDP18228D	256 X 4 CMOS	STATIC RAM	31 AUG 76	TEMP:	∍\$5 Ç	SN:	21
					PAGE	6 G F	10	
	000	001	nas	003				
A0H5 A0H7 A0F5 A0F7	100.MV 95.0MV 4.88 V 9.82 V	100, MV 105. MV 4,88 V 9,82 V	105.MV 115.MV 4.88 V 9.81 V	105,MV 115,MV 4,88 V 9,83 V				
ION1 IDN2 IDP1 IDP2	7,45MA 19,3MA -3,09MA -6,85MA	7,30MA 18,2MA -3,13MA -6,96MA	6.90MA 16.4MA ≈3.08MA ≈6.74MA	6,90MA 16,6MA 5,18MA 7,06MA				
1021 1022 1023 1024	6,90NA 2,80NA 1,10NA 4,60NA	-1.30NA 600.PA 3.20NA -200.PA	5.80NA 3.40NA -600.PA 3.00NA	=1,40NA =500.PA 3,90NA 700.PA				
1025 1026 1027 1028	400,PA 400,PA 500,PA 600,PA	2,70NA 3,00NA 2,50NA 2.80NA	800,PA 900.PA 900.PA 1.10NA	ANRS,S ANRO,S ANRO,I				
ILOP	-10.0UA							
IL1 IL2 IL3 IL4	-5.00UA -5.00UA -5.00UA -5.00UA							

RCA CDP18225D 256	X 4 CMOS STA	ITIC RAM	31 AUG 78 YE	MP: 85 C S
i			P	AGE T OF 10
PASSED GALPAT (WIDE PASSED GALPAT (TIGHT PASSED GALPAT (TIGHT	T LIMITS) VC	C=10V C=10V C=5V	REPRODUCIBILIT ORIGINAL PAGE	
PASSED DATA RETENTION	N TEST			
	vcc	= 4.5V	5 . 0v	10.0V
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA) (TDS) (TDH)	289.N 26.0N 16.0N	240' N 22 m n 14 m n	1 4 ° 6 M 1 6 ° 6 M 1 6 ° 9 M
ADDRESS SETUP TIME ADDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WIDTH	(TAS1) (TAS2) (TAH) (TWP)	10.0N 140.N =20.0N =6.0N	10.0N 122.N -16.0N 78.0N	6.00N 64.0N -6.00N 44.9N
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TC881) (TC882) (TC8H1) (TC8H2)	196.N 190.N 52.0N 56.0N	168, N 166, N 46, AN 50, AN	86, 8N 86, 8N 88, 9N 88, 8N
OUTPUT ACTIVE FROM CS OUTPUT ACTIVE FROM MS OUTPUT ACTIVE FROM MS	(SADOT) SE	270, N 266. N 64. ØN	236, N 232. N 56. ØN	125.N 12.0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH1) (TDOH2) (TDOH3) (TPOH) (TRC) (TWC)	166 N 162 N 146 N 144 N 309 N 264 N	130°N 130°N 130°N 130°N 130°N 130°N 130°N	46,2N 46,2N 38,2N 42,2N 138,N
IIL	ITH	VICI	VICE	
A0 =19,2NA A1 =18,8NA A2 =18,0NA A3 =22,0NA	18.5NA 18.4NA 18.2NA 18.4NA	3,15 V 3,15 V 3,18 V 3,17 V	#3,18 V #3,19 V #3,19 V	
A4 =18,4NA A5 =18,9NA A6 =18,4NA A7 =18,1NA	18,5NA 18,5NA 21.0NA 19.4NA	3.20 V 3.11 V 3.09 V 3.11 V	#3,17 V #3,13 V #3,15 V #3,13 V	
CS1 =19,3NA CS2 =19,2NA MWR =17,7NA MRD =18.6NA	18.4NA 20.2NA 17.5NA 18.6NA	3,13 V 3.16 V 3.11 V 3.12 V	#3/15 V #3/15 V #3/13 V	
DIO =19,1NA DI1 =20,6NA DI2 =18,1NA DI3 =18,8NA	20,4NA 19,2NA 19,7NA 19,5NA	3.20 V 3.21 V 3.20 V 3.17 V	#3,19 V #3,19 V #3,15 V	

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RCA	CDP1822SD	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP	85 C	SNI	21
					PAGE	8 OF	10	
:	npø	001	noe	003				
00H2	140 MY 145 MY 4 80 V 9 71 V	145.MV 155.MV 4.80 V 9.72 V	150,MV 175,MV 4.79 V 9.70 V	155,MV 175.MV 4,80 V 9,72 V				
IDN1 IDN2 IDP1 IDP2	5,35MA 13,2MA =1,91MA =4,31MA	5.20MA 12.2MA -1.96MA -4.37MA	4.90MA 11.0MA -1,80MA -4.17MA	4.90MA 11.2MA -1.94MA -4.40MA				
1071 1072 1073 1074	337.NA 327.NA 330.NA 323.NA	323,NA 330,NA 324.NA 330.NA	301,NA 29,NA 300,NA 302,NA	328, NA 321, NA 326, NA 320, NA				
1025 1026 1027 1028	327.NA 331.NA 337.NA 327.NA	332,NA 327,NA 323,NA 332,NA	304.NA 315.NA 307.NA 306.NA	331.NA 320,NA 329,NA 325.NA				
ILDP	-5.00UA							
IL1 IL2 IL3 IL4	⇔20,0UA ⇔25.0UA ⇔50.0UA ⇔45.0UA							

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RCA	CDP18228D	256 X	4 CMOS	STATIC RAM	31 AUG 78	ŸEMPÍ	iãs c	SNI	21
						PAGE	9 OF	10	
PASS	ED GALPAT ED GALPAT ED GALPAT	(TIGHT	LIMITS) LIMITS) LIMITS)	AGC=16A AGC=16A			•		

	• •			
	VCC	# 4.5V	5. øv	10.00
ADDRESS ACCESS TIME	CAAT	285.N	245 N	120 N
DATA SETUP TIME DATA HOLD TIME	(TDS) (TDH)	26,ØN 18,ØN	22.0N 16.0N	10,0N 16,0N
ADDRESS SETUP TIME	(TAS1)	8.00N	B DON	6. pon
ADDRESS SETUP TIME	(SEAT)	146 N -20 ØN	130°W	72.0N
ADDRESS HOLD TIME WRITE PULSE WIDTH	(TAH) (THP)	94.ØN	#18. ØN 84. ØN	#8,00N 45,0N
CS1 SETUP TIME	(TCSSÏ)	206.N	182, N	94. @N
CS2 SETUP TIME	(TCSS2)	202.N	176.N	94, ØN 92, ØN
CS1 HOLD TIME CS2 HOLD TIME	(TCSH1) (TCSH2)	56,0N 62.0N	50,0N 54.0N	30,0N 30,0N
OUTPUT ACTIVE FROM CS	1 (TDOAI)	286,N	250'N	130.N
OUTPUT ACTIVE FROM CS	(SAOOT) S	28g.N	246,N	128.N
OUTPUT ACTIVE FROM MR		68, ØN	60.0N	36 ON
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM CS2	(TDOH1) (TDOH2)	170.N 164.N	138, N 134, N	50,0N 50,0N
OUTPUT HOLD FROM MRD	(EHOOT)	146.N	124,N	50,0N 30,0N 40,0N
OUTPUT HOLD FROM MWR READ CYCLE TIME	(TPDH) (TRC)	148 "N 312 "N	124 N 272 N	40,0N 136,N
WRITE CYCLE TIME	(TWC)	280.N	240.N	158 N
ii.	IIH	VICI	VICE	
	102.NA	3,14 V	23,11 V	
	99.5NA 99.7NA	3,14 V 3,18 V	#3,19 V #3,19 V	
	102.NA	3,18 V 3.16 V	93,19 V 93,19 V	
A4 =104.NA	101, NA	3,20 V	-3,17 V	
A5 =106.NA	101 NA	5.09 V	A تروق	
A6 -105.NA A7 -104.NA	106,NA 104,NA	3.10 V	-3,14 V -3,12 V	
CS1 =110 NA	102,NA	3,13 V	-3,14 V	
CS2 #109.NA	107.NA	3,15 V	-3,15 V	
MWR #104,NA ************************************	99.4NA 103.NA	3.10 V 3.10 V	73,14 V 73,15 V 73,15 V 73,15 V	
DIO #105.NA	126 NA	3.20 V		
DI1 #111.NA	106, NA 105, NA 105, NA	3,20 V	.3,13 V	
DI2 -103.NA	105.NA	3,19 V	#3,19 V #3,13 V #3,14 V #3,13 V	
DI3 -105.NA	105.NA	3.17 V	#5.15 V	

RCA	CDP1822SD	256 >	(4	CMOS	STATIC	RAM	31	AUG	78	TEMPI	125	С	SNI	21
										P4GF	10	OF	10	

	DOØ	001	poe	DN3
AOH5 AOF5 AOF7	155.MV 165.MV 4.77 V 9.68 V	160,MV 175.MV 4,77 V 9,68 V	170.MV 200.MV 4.76 V 9.66 V	170 MV 195 MV 4,78 V 9,68 V
ION1 IOP1 IOP2	4.80MA 11.7MA ≈1.73MA ≈3.88MA	4.70MA 10.9MA ∞1.75MA -3.91MA	4.40MA 9.75MA ≈1.68MA ÷3.73MA	4,40MA 9,95MA =1,77MA =3,96MA
1021 1022 1023 1024	1.43UA 1.42UA 1.42UA 1.42UA	1,38UA 1,38UA 1,37UA 1,37UA	1.31UA 1.31UA 1.32UA 1.31UA	1,37UA 1,38UA 1,37UA 1,38UA
1025 1026 1027 1028	1.43UA 1.44UA 1.44UA 1.42UA	1.39UA 1.39UA 1.39UA 1.39UA	1.34UA 1.34UA 1.33UA 1.32UA	1,41UA 1,39UA 1,39UA 1,40UA
ILDP	15.0HA			
ILI IL2 IL3 IL4	AUQ.08= AUQ.09= AU,051= AU,201=			

RCA	CDP16288D	856 X 4	CMOS STATEC RAM	31 AUG 78	TEMP	85 C 8N8	22
					pies	1 AF 18	

PASSED GALPAT (TIGH	T LIMITS) VČ(T LIMITS) VČ(C=10V C=10V C=5V	REPRODUCIBE ORIGINAL PA	
PASSED DATA RETENTIO		¤ 4.5∨	5 . 0V	10°.00
		- 		
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	CAA7) CBOT) CHOT)	225,N 26,0N 10,0N	195 N 20 N 10 N	12.0N 12.0N 12.0N
ADDRESS SETUP TIME	(TAS1)	14, ØN	10,0N	4.00N 48.0N
ADDRESS SETUP TIME ADDRESS HOLD TIME	(TASE) (Hah)	112.N -18.0N 76.0N	_98 _≖ 0N +14 _≠ 0N	#4.92N
WRITE PULSE WIDTH	(TWP)	76,0N	68 * QN	38 QN
CS1 SETUP TIME	(TCSSI)	170.N	146 N	72,0N 70,0N 26,0N
CSS SETUP TIME CS1 HOLD TIME	(TC882) (TC8H1)	165 N 50, ØN 54. ØN	142.N 46.ON	\$ 6 \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
CS2 HOLD TIME	(TCSH2)	54.ØN	46. AN	26,0N
OUTPUT ACTIVE FROM C		216.N	188 N 184 N	94 gN
• · · · · · · · · · · · · · · · · · · ·	S2 (TDOA2) RD (TAOA3)	214.N 50.0N	184.N 44.DN	90,0N 26,0N
OUTPUT HOLD FROM CS1	(TDOH1)	<u>1</u> 42.N	i į s', N	34,0N
OUTPUT HOLD FROM CSE	(\$DOH2)	140 N	110.N	34,0N
OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR	(T00H3) (HD47)	138.N 132.N	116,N 112,N 208,N	32.0N
READ CYCLE TIME WRITE CYCLE TIME	(TRE) (TWC)	240 N 224 N	208, N 200. N	120.N 112.N
	_			14581
IIL	ITH	VICI	VICE	
AO -3.70NA A1 -3.70NA	3,50NA	3,30 V 3.32 V	-3,30 V -3,35 V	
A2 -3,40NA	3,80NA 3,20NA	3,34 V	,3,36 V	
A3 =3.60NA	3,00NA	3.30 V	~5.34 V	
A4 -3.00NA	2,60NA	3,29 V	₹3,30 V	
A5 =4.30NA A6 =4.90NA	4,10NA 5,00NA	3.35 V 3.37 V	•3,38 V •3,40 V •3,45 V	
A7 -5.70NA	4.90NA	3.41 V	=3'45 V	
CS1 #3.50NA	3,30NA	5.30 V	-3,30 V	
CS2 =3.50NA MWR =3.10NA	3,50NA 2,90NA	3,34 V 3,22 V	#3,38 V #3,24 V #3,28 V	
MRD =3.30NA	3.10NA	3.27 V	#3,28 V	
DIO -5,20NA	5,30NA	3,53 V	-3,49 V	
DI1 -5.30NA DI2 -4.30NA	5,10NA 4,10NA	3.49 V 3.46 V	#3,44 V #3,40 V #3,40 V	
DI3 =4.10NA	3.90NA	3.45 V	=3.40 V	

RCA	CDP18225D	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP	25 C SN:
					PAGE	2 OF 10
	סמס	001	poa	003		,
AOH5 AOH1 AOF5 AOF1	100,MV 110.MV 4,84 V 9,77 V	105, MV 125, MV 4,84 V 9,77 V	110,MV 140,MV 4,84 V 9,76 V	110, MV 135, MV 4,84 V 9,77 V		
IDN1 IDN2 IDP1 IDP2	7,45MA 17,2MA +2,43MA +5,43MA	7.05MA 15.4MA -2.47MA -5.47MA	6.65MA 13.8MA -2.43MA -5.30MA	6 65MA 14 0MA -2 46MA -5 49MA		•
1021 1022 1023 1024	138.NA 131.NA 135.NA 127.NA	120, NA 126, NA 123, NA 130, NA	107.NA 102.NA 103.NA 103.NA	101, NA 101, NA 104, NA 100, NA		
1025 1026 1027 1028	135.NA 128.NA 134.NA 135.NA	125, NA 128, NA 119, NA 124. NA	106.NA 110.NA 115.NA 105.NA	108 NA 97 6NA 98 4NA 106 NA		
ILDP	-5 .00UA					
IL1 IL2 IL3 IL4	-5.00UA -10.0UA -10.0UA -10.0UA					

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RCA CDP1822SD 256 X 6 CMOS STATIC RAM 31 AUG 78 TEMP1 WES C SN: 22

PASSED G	ALPAT	(WIDE	LIMITS	VCC=10V		
PASSED G	ALPAT	(TIGHT	LIMITS	VCC#10V	REPRODUCIBILITY OF TH	HE.
PASSED G	· · ·	-		VCC=5V	ORIGINAL PAGE IS FOO!	r.

	VCC	= 4 ₌ 5V	5,0V	10'.0V
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA) (807) (HDT)	25 ° N 26 ° N 8 ° DON	190 N 20 ON 10 ON	75.0N 8.00N 10.0N
ADDRESS SETUP TIME ADDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WIDTH	(TAS1) (TAS2) (TAH) (TWT)	20.0N 108.N -16.2N 72.0N	14,0N 90,0N -12.0N -60,0N	4 . 00 N 42 . 0 N 4 4 . 00 N 3 4 . 0 N
CS: SETUP TIME CS: SETUP TIME CS: HOLD TIME CS: HOLD TIME	(TCSS) (TCSS2) (TCSH1) (TCSH2)	166 a N 162 a N 40 a O N 42 a O N	140, N 136, N 36, GN 38, GN	06,00 64,00 82,00 22.00
OUTPUT ACTIVE FROM CS1 OUTPUT ACTIVE FROM CS2 OUTPUT ACTIVE FROM MRD	(TDGA2)	210.N 208.N 44.0N	178, N 176, N 40, AN	84,2N 82,0N 24.0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOMI) (TDOME) (TDOME) (TPOM) (TRC) (TWC)	136 ° N 136 ° N 136 ° N 132 ° N 240 ° N	106, N 106, N 114, N 108, N 200, N 184, N	30,00 30,00 30,00 30,00 112,0 112,0
IIL I	IH	AICT	VICZ	
A1 =300.PA 4 A2 =300.PA 3	00, PA 00, PA 00, PA 00, PA	3.26 V 3.28 V 3.30 V 3.27 V	03,26 V V 02,26 V 12,26 V 02,26	
A5 -400 PA 4 A6 -500 PA 5	00'PA 00'PA 00'PA 00'PA	3.27 V 3.29 V 3.30 V 3.34 V	-3,28 V -3,32 V -3,34 V -3,36 V	
CS2 -400 PA 4	00,PA 00,PA 00,PA 00.PA	3,27 V 3,30 V 3,21 V 3,25 V	.3,27 V .3,34 V .3,23 V .32,26 V	
DI1 =500.PA 4 DI2 =400.PA 4	00, PA 00, PA 00, PA 00, PA	3,45 V 3,42 V 3,40 V 3,38 V	#3,41 V #3,37 V #3,34 V #3,34 V	

RCA	CDP1822SD	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP	-20 C SN:
					PAGE	4 OF 10
	000	001	noŝ	003		
AOH 5 AOH 7 AOF 5 AOF 1	85.0MV 95.0MV 4.87 V 9.81 V	90.0MV 105.MV 4.87 V 9.81 V	95.0MV 120.MV 4.86 V 9.80 V	95 AMV 115 MV 4587 V 9581 V		
10N1 10P1 10P2	8 40MA 19 6MA = 2 89MA = 6 41MA	8,00MA 17,8MA -2,93MA -6,45MA	7.55MA 16.0MA -2.88MA -6.30MA	7,60MA 16,1MA -2,95MA -6,52MA		
1071 1072 1073 1074	13.6NA 16.5NA 11.0NA 10.1NA	13.2NA 9.90NA 14.5NA 15.9NA	10,2NA 13.4NA 9.40NA 7.40NA	11 4NA 8.10NA 10.6NA 13.4NA		
1025 1026 1027 1028	17,3NA 17,4NA 17,5NA 17,2NA	8,90NA 9,30NA 9,20NA 9,20NA	15,1NA 15,2NA 14,6NA 14,5NA	7,10NA 6,90NA 7,10NA 7,20NA		
ILOP	3,40UA					
11.1 11.2 11.3 11.4	-5.00UA -5.00UA -5.00UA -5.00UA	·				

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RCA COP18228D 256 X 4 CMOS STATIC RAM 31 AUG 76 TEMP1 -55 C SN1 22

PASSED GALPAT (WIDE LIMITS) VCC=10V PASSED GALPAT (TIGHT LIMITS) VCC=10V PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

LMOOFD DAIN WEIENITH	1501			
	VCC	¤ 4 _a 5y	5,ø∨	10.0v
ADDRESS ACCESS TIME	(TAA)	n.ess	180 k	70.9N
DATA SETUP TIME	(TDS)	ng.se	24 m on	8.90N
DATA HOLD TIME	(TDH)	ngg.a	8 m oon	10.9N
ADDRESS SETUP TIME	(TAS1)	18 pn	12,0N	4.00N
ADDRESS SETUP TIME	(TAS2)	102 n	84.0N	38.0N
ADDRESS HOLD TIME	(TAH)	16 on	*12.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	78 on	64.0N	32.0N
C81 SETUP TIME C82 SETUP TIME CS1 HOLD TIME C82 HOLD TIME	(TCSS1) (TCSS2) (TCSH1) (TCSH2)	160 N 154 N 44 2 N 46 2 N	130 N 128 N 38 ON 38 ON	60,0N 60,0N 60,0N
OUTPUT ACTIVE FROM CS OUTPUT ACTIVE FROM MR	(SAODT) SI	202.N	168° N 164° N 36° MN	84,0M 82,0N 22,0N
OUTPUT HOLD FROM CS: OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH!) (TDOH2) (TDOH3) (TPOH) (TRC) (TWC)	130 m 128 m 134 m 130 m 130 m 130 m 130 m 130 m 130 m	100°N 100°N 112°N 108°N 192°N 184°N	28
IIL	IIH	VICI	VICE	
A0 +100.PA	100,PA	3.27 V	+3,26 V	
A1 +100.PA	100,PA	3.29 V	+3,31 V	
A2 +100.PA	100,PA	3.31 V	+3,32 V	
A3 +100.PA	100,PA	3.28 V	+3,31 V	
A4 =100,PA	100 PA	3'.29 V	3,32 V	
A5 =100,PA	100 PA	3,29 V	3,32 V	
A6 =100,PA	100 PA	3,30 V	3,34 V	
A7 =100,PA	100 PA	3.34 V	3,37 V	
CS1 =100.PA	100, PA	3,28 V	73,28 V	
CS2 =100.PA	100, PA	3,31 V	73,35 V	
MWR =100.PA	100, PA	3,24 V	83,25 V	
MRD =100.PA	100, PA	3,26 V	83,27 V	
DIO =100.PA	100,PA	3,44 V	-3,40 V	
DII =100.PA	100,PA	3,41 V	-3,36 V	
DI2 0.00 A	100,PA	3,39 V	-3,33 V	
DI3 =100.PA	100,PA	3.38 V	-3,32 V	

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RCA	CDP1822SD	256 X 4	CMOS STATIC RAM	31 AUG 78	TEMP:	#55 C S	N: 22
					PAGE	6 OF 10	

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	noø	001	nor	003
			ı	
VOL1	80,0MV	85.0MV	85 . 0MV	85.9MV
AOLS	85.0MV	95.0MV	105.HV	105.MV
VOHI	4.88 V	4_89 V	4'.a8 v	105.MV 4.85 V
VOHE	9.84 V	9.84 V	9.83 V	9 84 V
V 45 * * 14		* B W = r · ·	7 # 17 # 7	1 E O - 7
IDN1	9,25NA	8.85MA	8.40MA	8 40MA
IDNS	21,8MA	19.9MA	18.0MA	
				_15 RMA
IDPI	#3.36MA	-3.40MA	-3-38MA	#3,44MA
IDP2	-7. 39MA	-7 . 44MA	+7.31MA	-7.54MA
	4			
1021	6.80NA	100.PA	5.10NA	400 PA
Ioza	5,60NA	-600.PA	5.70NA	=1,30NA
1023	-100 PA	5,70NA	-1.20NA	5,70NA
1074	3.00NA	2.80NA	1.10NA	3,30NA
7-	-			
1025	3.70NA	900 PA	3.80NA	-100 PA
1076	3.60NA	1.30NA	4.00NA	-400 PA
1027	3.80NA	800.PA	4,00NA	-200.PA
	_		•	
1028	3,70NA	1.10NA	4 . 1 ØN A	#500_PA
TI NO	TAB. N.A.			
ILDP	-200 NA			
41.4	E malla			
IL!	⇔5.ØØUA			
irs	⇔5,00UA			
IL3	- 5_00UA			
IL4	⇔5 ,00UA			
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PAGE 7 OF 10

PASSED	GALPAT GALPAT GALPAT	(TIGHT	LIMITS	VCC=10V VCC=10V VCC=5V	REPRODUCIBILITY ORIGINAL PAGE I	
PASSED	CATA RET	ENTION	TEST			
				466 - # 64	ຣ່ ຜນ	ta a.

PASSED GATA RETENTION	1521			
	VCC	= 4.5V	5'.ØV	10'.0V
ADDRESS ACCESS TIME	(TAA)	225.N	aud'n	95 <u>,</u> 0N
				8 60N
DATA SETUP TIME	(TDS)	28.0N	22.0N	12.0N
DATA HOLD TIME	(TDH)	12.ØN	12.78	12.00
ADDRESS SETUP TIME	(TAS1)	8.00N	B ู้ ØØN	4.00N
ADDRESS SETUP TIME				56.0N
	(TAS2)	120 N	196.N	
ADDRESS HOLD TIME	(TAH)	-18.0N	-16.PN	∞4.00N
WRITE PULSE WIDTH	(TWP)	86.0N	78.0N	44 20 N
CS1 SETUP TIME	(TCSS1)	180.N	156, N	80,0N
CS2 SETUP TIME	(TCSS2)	174.N	152.N	78, ØN
CS1 HOLD TIME	(TCSH1)	58, ØN	50.0N	30,0N
CS2 HOLD TIME	(TCSH2)		54. MN	30.0N
cos noto tine	((Cane)	60.0N	34 • WM	ייומ פשב
OUTPUT ACTIVE FROM CS1	(TDOA1)	228.N	290,N	126.N
OUTPUT ACTIVE FROM CS2		224.N	198.N	104 N
OUTPUT ACTIVE FROM MRD		54 UN	50.0N	30.0N
adiral adiate real top	(15075)	744 B 1214	2	2010
OUTPUT HOLD FROM CS1	(TDOH1)	148.N	118 N	38,0N
OUTPUT HOLD FROM CS2	(SHOOT)	146.N	116 N	38, ØN
OUTPUT HOLD FROM MRD	(TDOH3)	140.N	118 N	34,0N
OUTPUT HOLD FROM MWR	(TPDH)	136.N	144 N	36.0N
READ CYCLE TIME	(TRE)	248 N	224,N	128,N
WRITE CYCLE TIME	(TWC)	232.N	208.N	128.N
HATTE GIVER 120E	(1116)	20E • W	E & D * M	150.10
IIL I	.IH	VICI	AICS	
AØ -58,7NA 5	8.9NA	3,36 V	-3,36 V	
	7.2NA	3.38 V	-3,40 V	
•	1.0NA	3.38 V	#3.41 V	
	18.7NA	3.35 V	+3,41 V +3,38 V	
		3 E 3 D T		
A4 -44.8NA 4	12.5NA	3.32 V	-3,34 V	
-	8.3NA	3.41 V	-3,44 V	
	4.5NA	3.44 V	-3,47 V	
A7 -90.2NA 8	4.6NA	3.49 V	-3,53 V	
· ·				
	IO.9NA	3,35 V	-3,35 V	
	5.7NA	3,39 V	-3,44 V	
	14.5NA	3.86 V	-3,28 V	
MRD #49,7NA 4	AMS.BI	3.31 V	≈3.33 V	
entwent day, levels	Long diskut		*_*	
• • • • • • • • • • • • • • • • • • •	19.6NA	3.62 V	3,59 V	
	34.4NA	3,58 V	₩3,52 V	
	1.8NA	3.54 V	=3,48 V	
DI3 =69.1NA 6	9.6NA	3,52 V	=3,47 V	

RCA	CDP1822SD	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP:	85 C SN:
					PAGF	8 OF 10
	000	DO1	poe	003		
VOL 1 VOH 1 VOH 2	115.MV 130.MV 4.81 V 9.72 V	125,MV 145,MV 4,81 V 9,72 V	135.MV 165.MV 4.80 V 9.72 V	130.MV 165.MV 4,81 V 9,73 V		
IDN1 IDN2 1901 S901	6.35MA 14.6MA #2.05MA #4.57MA	6.00MA 13.1MA -2.07MA -4.59MA	5_65MA 11_7MA =2_02MA =4_44MA	5.65MA 11.8MA -2.09MA -4.63MA		
IOZ1 IOZ2 IOZ3 IOZ4	1.45UA 1.46UA 1.45UA 1.46UA	1,37UA 1,36UA 1,38UA 1,37UA	AU15.1 AU15.1 AU15.1 AU55.1	1,10UA 1,09UA 1,11UA 1,10UA		
1025 1026 1027 1028	1.47UA 1.48UA 1.47UA 1.48UA	1,41UA 1,41UA 1,40UA 1,39UA	1.24UA 1,23UA 1.23UA 1.23UA	1,15UA 1,12UA 1,12UA 1,11UA		
ILDP	13.201					
IL1 IL2 IL3 IL4	-45,0UA -50,0UA -50,0UA -45,0UA					

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PASSED	GALPAT	(WIDE	LIMITS)	VCC=10V
PASSED	GALPAT	THRIT	LIMITS)	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS	VCC≈5V

(KODED	DATA REFERENCE	1 1401			
		VCC	* 4.5V	5,0V	10.0V
DATA SE	S ACCESS TIME ETUP TIME OLD TIME	(TAA) (TDS) (TDH)	245.N 28,0N 14.0N	215' N 24 - MN 14 - MN	105.N 10,0N 14.0N
ADDRESS ADDRESS	S SETUP TIME S SETUP TIME S HOLD TIME PULSE WIDTH	(TAS1) (TAS2) (TAH) (TNP)	8.00N 134.N -20.0N 94.0N	6,00N 118,N -18,0N 84,0N	4.00N 64.0N -6.0N 46.0N
CS2 SE	ETUP TIME ETUP TIME OLD TIME	(TCSS1) (TCSS2) (TCSH1) (TCSH2)	190.N 188.N 60,0N 62.0N	166, N 164, N 54. ØN 56. ØN	88,0N 86,0N 32,0N 30,0N
OUTPUT	ACTIVE FROM CS ACTIVE FROM MR	(SAOUL) S	256.N 254.N 60.0N	226.N 224.N 54.0N	122.N 122.N 32.ON
OUTPUT OUTPUT OUTPUT READ C	HOLD FROM CS1 HOLD FROM CS2 HOLD FROM MRD HOLD FROM MWR YCLE TIME CYCLE TIME	(TDOH1) (TDOH2) (TDOH3) (TPOH) (TRC) (TWC)	154.N 150.N 140.N 138.N 264.N 248.N	124, N 122, N 120, N 116, N 240, N	44 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
	IIL	IIH	VICI	vica	
A0 A1 A2 A3	=349.NA =338.NA =313.NA =300.NA	346.NA 329.NA 299.NA 284.NA	3,46 V 3,47 V 3,48 V 3,43 V	#3,46 V #3,50 V #3,50 V #3,47 V	
A4 A5 A6 A7	#263.NA #412.NA #457.NA #520.NA	248.NA 399.NA 438.NA 498.NA	3.40 V 3.52 V 3,57 V 3.63 V	-3,41 V -3,56 V -3,60 V -3,66 V	
CS1 CS2 MWR MRD	~314.NA ~325.NA ~268.NA ~292.NA	295,NA 326,NA 252,NA 279,NA	3,44 V 3,48 V 3,33 V 3,40 V	23,44 V 23,54 V 23,35 V 23,41 V	
DIO DIA DIS	#504.NA #496.NA #417.NA #412.NA	521, NA 499, NA 420, NA 412. NA	3.76 V 3.71 V 3.66 V 3.65 V	73,72 V 73,65 V 73,61 V 73,60 V	

RCA	CDP1822SD	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP:	125 C	SNI	55
	•				PAGE	10 OF	10	
	noa	D01	500	003				
VOL1 VOH1 VOH2	130.MV 145.MV 4.78 V 9.69 V	140, MV 165, MV 4,78 V 9,69 V	150.MV 185.MV 4.78 V 9.68 V	150,MV 185,MV 4,78 V 9,69 V				
IDN1 IDN2 IDP1 IDP2	5.65MA 13.0MA -1.83MA -4.09MA	5.35MA 11.6MA ~1.84MA ~4.09MA	5.00MA 10.3MA 1.83MA 73.99MA	5.05MA 10.5MA +1.87MA +4.14MA				
1021 1022 1023 1024	6.32UA 6.33UA 6.33UA 6.33UA	5,97UA 5,98UA 5,97UA 5,99UA	5.30UA 5.30UA 5.32UA 5.31UA	4,85UA 4,87UA 4,86UA 4,88UA				
1025 1026 1027 1028	6.49UA 6.43UA 6.39UA 6.37UA	6,05UA 6,06UA 6,04UA 6,04UA	5.43UA 5.38UA 5.36UA 5.35UA	4,99UA 4,91UA 4,91UA 4,91UA				

80°0UA

-240.UA -240.UA -240.UA

ILDP

IL1 IL2 IL3 IL4 2.6

RCA CDP1822SD 256 X 4 CMOS STATIC RAM 31 AUG 78 TEMP: 25 C SN:	5.8
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PAGE 1 OF 10

PASSED GALPAT	(WIDE LIMITS) (TIGHT LIMITS) (TIGHT LIMITS)	VCC=10V	REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR
•	-		MINISTER TAGE IS BINIS

PASSED DATA RETENTION	TEST			
	vcc	= 4.5V	5.ØV	10.0V
ADDRESS ACCESS TIME	(TAA)	335 N	265.N	95'. ØN
DATA SETUP TIME	(TDS)	335.N 24.ØN	50.0N	8 . 00N
DATA HOLD TIME	(TDH)	10.0N	10.0N	10.0N
DRIN HOLD 1280.	4.10113	10.004	光の着石は	10 4014
ADDRESS SETUP TIME	(TAS1)	10.0N	8.09N	4.90N
ADDRESS SETUP TIME	(TASE)	180 N	142.N	64.0N
ADDRESS HOLD TIME	(TAH)	-18,0N	-14.0N	-2.00N
WRITE PULSE WINTH	(TWP)	70.0N	60.0N	36.0N
AO. APELIA CELE	480 - 04 5	A 200 000 A.1	474	4 4 1 100 11
CS1 SETUP TIME	(TCSS1)	170 N	136 N	66,0N
CS2 SETUP TIME	(TCSS2)	166 N	134.N	64, ØN
CS1 HOLD TIME	(TCSH1)	40,0N	34.0N	22,0N
CS2 HOLD TIME	(TCSH2)	42.ØN	38.0N	55,00
OUTPUT ACTIVE FROM CS	1 (TDOA1)	314.N	256 N	104 N
OUTPUT ACTIVE FROM CS		312.N	254.N	102.N
OUTPUT ACTIVE FROM MR		52.0N	46.0N	26. ØN
QUTPUT HOLD FROM CS:	(TOOH1)	148.N	116 N	36, ØN
OUTPUT HOLD FROM CS2	(TDOH2)	146 N	114,N	36,0N
OUTPUT HOLD FROM MRD	(TDOH3)	140 N	118, N	30,0N
OUTPUT HOLD FROM MWR	(ተቀሰዛጎ	136.N	112,N	36,0N 30,0N
READ CYCLE TIME	(TRC)	312.N	256,N	112.N
WRITE CYCLE TIME	(TWC)	272.N	208'N	112.N
IIL	IIH	vici	AICS	
AOO =2.00NA	1,90NA	3.02 V	=3,04 V	
A1 -1.90NA	1.80NA	3.05 V	-3,09 V	
	1,80NA	3,08 V	-3-11 V	
	1.60NA	3.10 V	-3.12 V	
A4 =1,70NA	1,80NA	3.10 V	-3,14 V	
	2,50NA	3,06 V	-3,06 V	
	2.00NA	3.05 V	⊕3,08 V ⊕3,10 V	
A7 #2.50NA	2.10NA	3.08 V	#3,10 V	
CS1 #1,60NA	2,10NA	3,12 V	-3,11 V	
CS2 =2.20NA	1,90NA	3,13 V	#3,15 V	
	1.70NA	3.07 V	3,05 V	
	1.90NA	3.08 V	#3,10 V	
_			-	
DI0 #2,30NA	5.50NV	3.19 V	-3,13 V	
DI1 -2.00NA	2,10NA	3.18 V	-3 ₋ 13 V	
	2.90NA	3.18 V	=3,17 V	
	1.90NA	3.18 V	-3.13 V	

RCA	CDP1822SD	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMPÍ	25 C	SN:
					PAGE	2 OF	10
	DOØ	001	005	003			
00H2 VOL2 VOL1	105,MV 110,MV 4,85 V 9,78 V	110 MV 115 MV 4 84 V 9 78 V	120,MV 135,MV 4,84 V 9.77 V	115 MV 130 MV 4,84 V 9,78 V			
ION1 ION2 IOP1 IOP2	7 10MA 17 5MA -2 54MA -5 73MA	6.75MA 16.0MA -2.48MA =5.66MA	6.25MA 14.0MA +2.45MA +5.47MA	6.35MA 14.5MA -2,48MA -5.67MA			
1021 1022 1023 1024	29,3NA 25,8NA 28,6NA 31,1NA	ANP.ES ANP.65 ANP.ES ANZ.15	29,2NA 25,6NA 26,3NA 29,8NA	ANB BS AND ES AND ES AND 15			
1025 1026 1027 1028	24,2NA 24,9NA 24,8NA 24,7NA	28.0NA 28,2NA 27.8NA 27.6NA	24 INA 23 9na 24 2na 24 6na	26.5NA 25.6NA 25.2NA			
ILDP	5.50NV						
IL1 IL2 IL3 IL4	-15,0UA -20,0UA -10,0UA -20,0UA						

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PASSED	GALPAT	(WIDE	LIMITS	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS)	VCC×10V
PASSED	GALPAT	(TIGHT	LIMITS)	VCC=5V

	VEC	= 4,5V	5 . 0V	10.0V
ADDRESS ACCESS TIME	(TAA)	395.N	285 N	90'_0N
DATA SETUP TIME	(Ths)	28. ØN	25.WN	8 <u>.</u> 00N
DATA HOLD TIME	(TDH)	8.00N	8.00N	10.0N
ADDRESS SETUP TIME	(TAS1)	16.0N	15"bN	4 . ØØM
ADDRESS SETUP TIME	(TAS2)	194.N	150.N	65. QN
ADDRESS HOLD TIME	(TAH)	-18,ØN	-14.6N	-2.00N
WRITE PULSE WINTH	CTWP)	70.0N	58.0N	32.00
man to a forther warrant			-	
CS1 SETUP TIME	(TCSS1)	N.555	132.N	60,0N
CS2 SETUP TIME	(TCSS2)	sså.N	1 30 %	55 @N 60 @N
CS1 MOLD TIME	(TCSH1)	34.0N	30. an	55,00
CS2 HOLD TIME	(TCSH2)	40 ON	32.0N	50 <u>°</u> 0H
OUTPUT ACTIVE FROM CS1	(TODA1)	336.N	262 N	98, BN
GUTPUT ACTIVE FROM CS2	(SADOT)	334.N	260 N	98, ØN
OUTPUT ACTIVE FROM MRD	(TODA3)	50.0N	42.9N	24.ØN
	(reans)	367 2 10 11		
OUTPUT HILD FROM CS1	(TDOH1)	142.N	112 N	34 ØN 34 ØN
OUTPUT HOLD FROM CS2	(SHOOT)	140.N	108.N	34,0N
OUTPUT HOLD FROM MRD	(TDOH3)	138 N	116,N 112,N	28, ØN
OUTPUT HOLD FROM MWR	(TPDH)	136.N	112,N	30.0N
READ CYCLE TIME	(TRC)	312,N	248, N	104.N
WRITE CYCLE TIME	(TWC)	256.N	500.V	96, 0N
tti. II	EH	VICI	VICA	
A0 -300.PA 30	70.PA	3.10 V	-3-11 V -3-15 V	
	70.PA	3.12 V	-3-15 V	
	DO PA	3.14 V	-3,16 V	
	70.PA	3.16 V	-3,17 V	
THE TRUE THE		,, <u>,</u> , , , , , , , , , , , , , , , , ,		
	70.PA	3.16 V	-3,20 V	
	00.PA	3.13 V	43,13 V	
A6 4400,PA 30	70' PA	3,12 V	新田市工作 A	
	NO PA	3.13 V	-3.15 V	
CS1 =200.PA 50	NO PA	3,19 V	-3,17 V	
CS2 -500.PA 40	ag PA	3.20 V	-3,21 V	
	70 PA	3.14 V	-3,13 V	
	70 . P A	3.14 V	-3,16 V	
ाणकाल्यक्रमा चर्	rev∎1 m	~# r 7 ¥	- -	
DIØ =400.PA 30	70.PA	3.25 V	-3-19 V	
	30,PA	3.24 V	-3,18 V	
	70,PA	3.24 V	-3-55 V	
	00.PA	3,24 V	-3.18 V	
-				

RCA	CDP18225D	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP	₩20 C SN:
					PAGE	4 OF 10
	poø	001	002	003		
VOL 1	95.0MV	95.0MV	105,MV	105, HV		
AOLS	95,0MV	105.MV	120.MV	115.MV	•	
VOHI	4,87 V	4,87 V	4.86 V	115 MV 4 87 V		
AOH5	V \$8,0	9 82 V	9.81 V	9 88 V		
IDN1	7.85MA	7.45MA	6.95MA	7.0544		·
IDNS	19.8MA	18.3MA	16.0MA	16.5MA		
IDP1	∞2 ,96MΛ	-2,95MA	≈2_88MA	-2 90MA		
IDP2	-6.72MA	-6.69MA	#6.45MA	-6.66MA		
1071	9.30NA	2.00NA	6.70NA	2.30NA		
1025	8,90NA	600.PA	8.20NA	490.PA		
1023	S,30NA	7.60NA	1,20NA	7,8004		
IÚZ4	4.70NA	5.10NA	3 10NA	5,70NA		•
1025	6.80NA	2,40NA	6.80NA	1 DONA		
1026	7.10NA	ANDO.S	6.80NA	1,20NA		
I027	7.10NA	5.60NA	7.00NA	1,0004		
TOZB	7.10NA	1.80NA	6.80NA	1.10NA		

ILDP	-1,40UA
IL1	-15,0UA
IL2	-20,0UA
IL3	-5,00UA
IL4	-15,0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V PASSED GALPAT (TIGHT LIMITS) VCC=10V PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

	vcc	= 4.5V	5 . av	10'.0v
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA) (TDS) (TDH)	425.N 34.0N 6.00N	300'.N 24.0N 6.00N	85'.0N 8.00N 8.00N
AUDRESS SETUP TIME AUDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WINTH	(TAS1) (TAS2) (TAH) (TWP)	16.0N 205.N -18.0N 76.0N	10.9N 154.N =14.0N 66.0N	4.00N 60.0N -2.00N 32.0N
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS1) (TCSS2) (TCSH1) (TCSH2)	242.N 242.N 42.0N 48.0N	128'N 126'N 36.0N 38.0N	56,0N 56,0N 20,0N 18,0N
OUTPUT ACTIVE FROM CS1 OUTPUT ACTIVE FROM MRD	(TDOA1) (TDOA2) (TDOA3)	364.N 360.N 46.ON	266' N 264' N 40' N	96,0N 94,0N 22,0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	CTOOH1) (TOOH2) (TOOH3) (TPOH) (TRC) (TWC)	138 N 136 N 136 N 134 N 328 N 256 N	106, N 104, N 114, N 110, N 248, N 176, N	34,0N 32,0N 28,0N 30,0N 104,N 96,0N
III. II	тн	VICI	VIC2	
A1 =100.PA 10 A2 =100.PA 10	10.PA 10.PA 10.PA	3.17 V 3.19 V 3.21 V 3.23 V	73,18 V 73,23 V 73,24 V 73,25 V	
A5 ~100,PA 30 A6 ~100,PA 10	10,PA 10,PA 10,PA 10,PA	3.23 V 3.20 V 3.19 V 3.21 V	-3,27 V -3,20 V -3,21 V -3,25 V	
CS2 =100,PA 10 MWR =100,PA 10	10, PA 10, PA 10, PA 10, PA	3,26 V 3,27 V 3,22 V 3,22 V	-3,24 V -3,28 V -3,20 V -3,23 V	
DI1 =100.PA 10 DI2 =100.PA 10	00,PA 10,PA 10,PA 10,PA	3.32 V 3.31 V 3.31 V 3.32 V	#3,26 V #3,25 V #3,25 V	
		B-225		

RCA	CDP1822SD	256 X 4	CMOS STATI	C RAM	31 AU	3 78	TEMP:	#ŠS C	SN:	23
							PAGE	6 OF	10	

	ngø	001	noe	003
VOL1 VOL2 VOH1	85.0MV 85.0MV 4.89 V 9.84 V	90.0HV 95.0MV 4.88 V 9.84 V	100.MV 105.MV 4.88 V 9.84 V	95.0MV 105.MV 4.88 V 9.84 V
ION1 IOP1 IOP2	8,45MA 21.8MA +3,41MA =7,70MA	8,10MA 20,2MA AM8E,E- AM8A,7-	7.55MA 17.9MA -3.30MA -7.41MA	7,65MA 18,4MA 73,38MA 7,69MA
IOZ1 IOZ2 IOZ3 IOZ4	-700°PA -200°PA 4.40NA 1.10NA	ANDS.E ANDS.1- ANDS.1- ANDS.5	ANDR 1 = 1 = 1 = 1 = 1 = 1 = 1 = 1 = 1 = 1	4,90NA 4,60NA -1.90NA 700,PA
1025 1026 1027 1028	2,50NA 1,90NA 2,10NA 1,60NA	1,90NA ANDO,5 ANDS,5 ANOA	700.PA 809.PA 400.PA 500.PA	2,70NA 3,00NA 3,00NA 3,30NA
ILDP	-15.0UA			
IL1 IL2 IL3 IL4	-10,0UA -15,0UA -5,00UA -10,0UA			

RCA	CDP1822SD	256 X 4	CMOS STATIC RAM	31 AUG 78	TEMP:	85 C	SNI	92

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PASSED	GALPAT	(WIDE	LIMITS)	VCC=10V
PASSED	GALPAT	(TIGHT	(.IMITS)	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS)	VCC=5V

ENGLINATION DATE RESERVED	[20]			
	vac	* 4.5V	5',0V	10'.0V
ADDRESS ACCESS TIME	(TAA)	746 N	255 N	105.N
		310.N		
DATA SETUP TIME	(TDS)	24, ØN	20,0N	8.00N
DATA HOLD TIME	(TDH)	12.0N	10.0N	12.0N
ADDRESS SETUP TIME	(TAS1)	6.00N	6,00N	4.00N
ADDRESS SETUP TIME	(TAS2)		138.N	68, ØN
ADDRESS HOLD TIME	(TAH)	172.N -18,0N	#14.0N	+4.00N
WRITE PULSE WIDTH	(TWP)	80.0N	70.0N	40.0N
			ę.	,
CS1 SETUP TIME	(TCSS1)	166,N	142 N	70 , 0N
CS2 SETUP TIME	(TCSS2)	164.N	140 N	70,0N
CS1 HOLD TIME	(TCSH1)	50,0N	44,0N	26,0N
CS2 HOLD TIME	(TCSH2)	54.0N	46.AN	26.0N
CHITCHT APPTUR FORM ACC	/*no.43	706 1	254 <u>,</u> N	4 4 34 64
OUTPUT ACTIVE FROM CS1	(TDOA1)	300.N		114.N
OUTPUT ACTIVE FROM CS2	(SADOT)	596 N	250 N	114.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	54.ØN	48.AN	28.ØN
OUTPUT HOLD FROM CS1	(TDOH1)	150.N	120,N	40, 0N
OUTPUT HOLD FROM CS2	(TDOH2)	148 N	118 N	<u> </u>
OUTPUT HOLD FROM MRD	(TDOH3)	140 N	118,N	40,0N 34,0N
OUTPUT HOLD FROM MWR	(TPDH)	138,N	4 4 / N	34.ØN
READ CYCLE TIME	(TRC)	312.N	114 N	
WRITE CYCLE TIME	(TWC)		264 N	120,N
MATIC CICLE TIME	(: WI.,)	224.N	200'N	120.N
IIL	ГН	VICI	vica	
A0 -25,0NA 23	3,9NA	3.00 V	+3,02 V	
	3.0NA	3,03 V	-3.06 V	
	3.5NA	3,06 V	-3,06 V -3,09 V	
•	6NA	3.08 V	#3.10 V	
				
	I, tha	3.98 V	÷3,12 V	
	5,1NA	3.05 V	-3-04 V	
	1.6NA	3.03 V	-3,04 V -3,06 V	
A7 =27.6NA 25	5.3NA	3.05 V	∞3.08 V	
CS1 -23,9NA 26	4.1NA	3.11 V	-3,09 V -3,14 V -3,23 V	
CS2 +25.4NA 24	1,9NA	3.12 V	-3-14 V	
	5 6NA	3.04 V	# 3 O 3 V	
	5,4NA	3.05 V	-3.08 V	
	5.4NA	3.17 V	=3,12 V	
	4.8NA	3.17 V	⇔3,12 V	
	7.0NA	3.17 V	#3,15 V	
DI3 =24.8NA 24	4.2NA	3.17 V	#3.11 V	

RCA	CDP18225D	256 X 4 CMOS	STATIC RAM	31 AUG 78 T	EMP:	85 C	SNI	23
				1	PAGE	8 OF 10	Ø	ط ك
	Dog	001	noż	200				**************************************
VOL.1	120.MV	125,MV	140.MV	135, MV				
VOL2	125 MV	140.MV	160.MV	155,MV				7 :
SHOA	4.82 V 9.74 V	4,82 V 9,74 V	4.81 V 9.72 V	155 MV 4 81 V 9 74 V				र्ह के
IDN1	6.20MA	5.85MA	5_40MA	5.50MA			•	
IDNS	15.1MA	13,7MA	11.9MA	12.4MA				
1001	=2.15MA =4.86MA	-2,11MA	-8.06MA -0.63MA	-2,10MA				ŧ ;
IDP2	-4 " ODWY	-4.77MA	-4.63MA	=4.79MA				· · · · · · · · · · · · · · · · · · ·
TOZI	AM.SES	223, NA	219.NA	224,NA				
Ioze	855*NY	228,NA	219.NA	218,NA				
1023		225.NA	218,NA	540°NY				. :
I0Z4	219.NA	224.NA	221.NA	214.NA				
1025	221.NA	228, NA	AZZ.NA	222, NA				
1026	229 NA	219,NA	233,NA	215,NA				· · · · · · · · · · · · · · · · · · ·
1027	231.NA	224.NA	219.NA	227, NA				
1078	555*NV	225.NA	225.NA	215.NA				1.5
								÷
ILDP	3,20UA							- <u>'</u>
2L1	-35.0UA							e £
IT5	#45.0UA							* 4
IL3	≖25,0UA							: 1
IL4	≈35.0UA							4.5

PAGE 9 OF 10

PASSED	GALPAT	(WIDE	LIMITS)	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITSI	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS)	VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

	VCC	= 4,5V	5 . 0v	10.0V
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA) (TDS) (TDH)	305.N 24.0N 12.0N	255.N 20.0N 12.0N	110.N 8.90N 12.0N
ADDRESS SETUP TIME ADDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WINTH	(TAS1) (TAS2) (TAH) (TWP)	4.00N 170.N •18,0N 84.0N	4.00N 148.N -14.2N 76.0N	4.00N 72.0N -4.00N 44.0N
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS1) (TCSS2) (TCSH1) (TCSH2)	170.N 166.N 52.0N 54.0N	150', N 146', N 46', QN 48', QN	78,0N 76,0N 28,0N 28.0N
OUTPUT ACTIVE FROM CS1 OUTPUT ACTIVE FROM CS2 OUTPUT ACTIVE FROM MRD	(TDOAZ)	306.N 304.N 58.0N	268'N 258'N 58'N	126.N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH1) (TDOH2) (TDOH3) (TPOH) (TRC) (TWC)	152 N 148 N 140 N 140 N 312 N 224 N	172, N 170, N 118, N 116, N 264, N	42,0N 42,0N 34,0N 38,0N 128,N
IIL	IH	VIC1	VICS	
A1 =144.NA 1 A2 =144.NA 1	38.NA 37.NA 37.NA 35.NA	3.00 V 3.03 V 3.07 V 3.09 V	-3,02 V -3,07 V -3,10 V -3,11 V	
A5 =145.NA 1 A6 =147.NA 1	38, NA 39, NA 43, NA 43, NA	3.08 V 3.05 V 3.04 V 3.06 V	-3,13 V -3,04 V -3,06 V -3,09 V	
CS2 =146.NA 1 MWR =139.NA 1	37.NA 41,NA 35,NA 35.NA	3,11 V 3,13 V 3,04 V 3,05 V	-3,09 V -3,14 V -3,03 V -3.08 V	
DI1 #143,NA 1 DI2 #142,NA 1	46, NA 43, NA 43, NA 40. NA	3.19 V 3.18 V 3.17 V 3.17 V	#3,15 V #3,13 V #3,16 V #3,12 V	

RÇA	CDP18228D	256 X 4	CMOS STATIC	RAM 31	AUG 78	TEMP:	125 C	SN:	23
						PAGE	10 OF	10	er g
	DOØ	DOi	200		EDG				

	DOØ	DO:	005	200
VOL1	130,MV	140 MV	155.MV	150, MV
VOL2	140,MV	155 MV	180,MV	175, MV
VOH1	4,80 V	4 80 V	4.78 V	4,79 V
VOH2	9,72 V	9 70 V	9.69 V	9,71 V
IDN1	5.60MA	5.30MA	4.85MA	4,95MA
IDN2	13.5MA	12.2MA	10.6MA	11,1MA
IOP1	-1.94MA	-1.91MA	=1.87MA	71,91MA
IDP2	-4.36MA	-4.30MA	=4.15MA	74,31MA
1021	895.NA	890, NA	885,NA	884, NA
1022	877.NA	883, NA	883,NA	875, NA
1023	875.NA	884, NA	878,NA	879, NA
1024	872.NA	875, NA	883.NA	873, NA
1025	880 NA	888,NA	895.NA	890, NA
1026	889 NA	878,NA	892.NA	884, NA
1027	883 NA	883,NA	881.NA	886, NA
1028	879 NA	877.NA	891.NA	875, NA
ILDP	40 mul			
IL1 IL2 IL3 IL4	-105.UA -135.UA -95.0UA	,		

RCA CDP1822SD 256 X 4 CMOS STATIC RAM 31 AUG 78 TEMP: 25 C SN: 26

PASSED GALPAT (WIDE LIMITS) VCC=10V PASSED GALPAT (TIGHT LIMITS) VCC=10V PASSED GALPAT (TIGHT LIMITS) VCC=5V

LMOOFD	DATA RETENTION	1 1 1 0 1						
			VCC	= 4 <u>*</u> 5	5 V	5.	ø۷	10°.00
ADDRESS	ACCESS TIME	{TAA	1	239	8 N	4.0	5 N	80°,0N
	ETUP TIME	(TDS			ØN		_ON	8 . ØØN
	JLD TIME	(103 HQT)			ØN		ON	16.QN
и міжа	arn itur	1,011	,	٠,	, gjirt	7 **	₩ 2)1V	T th * file
ADDRESS	S SETUP TIME	(TAS		iø.	ØN	10	" ØN	4 . ØØN
ADDRESS	S SETUP TIME	(TAS	2)	114	1 • N	96	_ 0 N	44, DN
ADDRESS	S HOLD TIME	НАТ))	-16,	ØN	-12	_ ØN	-2 °00N
WRITE F	PULSE WIDTH	(TWP)	62,		56	. ØN	34.0N
CS1 SE	ETUP TIME	(TCS	647	150	a ai	12	Ø, N	66', ON
	ETUP TIME	(TCS		148			8 N	64 ØN
	OLD TIME	(TCS		34/			• QV	22, 0N
CS2 HO	OLD TIME	(TCS	U5)	58.	.ØN	56	• NN	50.0N
กมระบา	ACTIVE FROM CS	31 (700	A 1 1	221	ı M	10	۵ <mark>م</mark> ۵	55, ØN
	ACTIVE FROM CS			224	•			88, ØN
	ACTIVE FROM ME				, ØN		8.N	26.0N
POTPOT	WELTAS LUM MI	יט נוטט	W D J	40,	ייינש ,	45	. an	E Ø•₩W
OUTPUT	HOLD FROM CS1	סקד)	HIT	143	. N	11	ร'ุ่ท	34,0N
	HOLD FROM CS2	(דם ח		•	3 N	10	8, N	34, ØN
	HOLD FROM MRD	(TDO			3 N	9 4	6 N	30, 6N
-	HOLD FROM MUR	(TPD		•.•	i _n N	1 (n N	32.0N
	YCLE TIME	(TRC			h a N	20	Ø N R N	112.N
	CYCLE TIME					5, W	BN	
MUTIC:	BYCHE THEE	(TWC	,	200	3.N	1 /	6.N	112.N
	IIL	IIH		VIC1		VICE		
AØ	#1.10NA	900 PA		2.86	٧	-2,83	V	
A1	■1.4×1NA	1.30NA		2.87		-2 89	· V	
SA	-1.00NA	1,40NA		2.86		-2,89	V	
A3	-1.30NA	1.50NA		2.83		#2,89 #2,89	٧	
A 4	e1,00NA	1,70NA		2.88		-2.99	V	
A5	-1.20NA	1,00NA		18.5		-2,85 -2,83	V	
A6	-1.50NA	1,30NA		88,5	٧	-2,83	V	
A7	+1.20NA	1.30NA		8,80	٧	-2.85	ν	
CS1	-1.00NA	1,30NA		2.83	V	2,84	v	
css	-1.30NA	T P JOHN		2.86			Ÿ	
MWR	=	1.10NA		2.81		m2,86	V	
MRD	-1,40NA ≈1,60NA	900.PA				-2.81 -2.81	V	
CONTA	™ 1 9 ON IA W	1.00NA		2.84	7	-2.83	*	
DIØ	-1_60NA	1.00NA		2.89	٧	-2.84	. V	
DII	-1.10NA	1.00NA			Ÿ	~2,B3		
DIS	-1.50NA	1,10NA		2.89		#2,83		
013	-1.20NA	1.50NA		2.89		÷2.85		
~ 42 25	1 de 8 fan 841 778	P = -4.14 LA LA		g U /	•	~ H B U J	• •	

RÇA	CDP18225D	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP:	25 C	SN:	24
					PAGE	a of	10	
	DOM	001	paa	003				
VOL.1	105.MV	115, MV	ian,mv	120, MV				
AOFS	110.MV	125.MV	140 MV	140 MV				
VOH1	4.86 V	4,86 V	4.85 V	140 MV 4,85 V				
ADH5	9.78 V	9,78 V	9.77 V	9,78 V				
IDN1	6.90MA	6,55MA	6.20MA	6.20MA				
INNS	17.0MA	15.4MA	13.6MA	.13.8MA				
IDP 1	-2.67MA	-2.64MA	≈2.63MA	-2,64MA			•	
1065	-5.72MA	-5.72MA	-5.55MA	#5.73MA				
IOZ1	25.0NA	17.0NA	22,9NA	16.3NA				
1022		19.6NA	19,7NA	18,5NA				
1023	22.3NA	19.5NA	18,3NA	20,5NA				
1024	26.0NA	16.5NA	55.5NV	17,4NA				
1025	19.3NA	21,7NA	18,0NA	21.6NA				
1026	19,8NA	55.5VA	18,0NA	ANI.15				
1027	19,7NA	21.6NA	17,9NA	21.3NA				
1028	19.7MA	22.0NA	17.9NA	20.8NA				-
ILOP	~20.0UA							
ILi	≕30,0UA							
ILS.	=40,0UA							
IL3	-75,0UA							
11.4	-80.0UA							
7 th4	— an • n a v							

PAGF 3 OF 10

PASSED	GALPAT	(WIDE	LIMITS)	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS)	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS	VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION	TEST			
	VCC	≃ 4.5V	5 . øv	10.0V
ADDRESS ACCESS TIME	(AAT)	235.N	190.N	75.0N
DATA SETUP TIME	(TDS)	20,0N	16.0N	6.00N
DATA HOLD TIME	(ซกับ)	12,0N	12.0N	16. AN
	4		# to M 4.11	* * * *
ADDRESS SETUP TIME	(TAS1)	12'.ØN	10.0N	4.00N
AUDRESS SETUP TIME	(TASE)	112.N	92. NN	40 ON
ADDRESS HOLD TIME	(TAH)	-14,0N	#12.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	60.0N	60.QN	32.0N
With gade harry	4 · · · · · F			
CS1 SETUP TIME	(TCSS1)	142.N	155, N	65 BN
CS2 SETUP TIME	(TCSS2)	140 N	120 N	60,01
CS1 HOLD TIME	(TCSH1)	34,0N	30,0N	20,0N
CS2 HOLD TIME	(TCSH2)	36 0N	38.9N	PO ON
, , , , , , , , , , , , , , , , , , , ,	********		(merce major c. t	
OUTPUT ACTIVE FROM CS1	(TDOA1)	218.N	180 N	80 _គ ់ ØN
OUTPUT ACTIVE FROM CSa		218.N	178 N	80 QN
OUTPUT ACTIVE FROM MRD		42.0N	38. AN	80,0N 24.0N
		*		
OUTPUT HOLD FROM CS1	(TDOH1)	134.N	104, N	32,04
OUTPUT HOLD FROM CS2	(SHOOT)	132.N	102.N	32.0N
OUTPUT HOLD FROM MRD	(TDOH3)	136,N	114 N	28, ØN
OUTPUT HOLD FROM MWR	(TPDH)	132.N	110.N	30,0N
READ CYCLE TIME	(TRC)	224,N	\$00 N	96.0N
WRITE CYCLE TIME	(TWC)	200 N	114, N 110, N 200, N 168, N	104.N
IIL I	[TH	VIC1	AICS	
	•			
	00 PA	3,00 V	≟2,96 V	
	200,PA	3.00 V	73°05 ∧	
	90,PA	5°33 A	-3,02 V	
A3 #200,PA &	200.PA	2.97 V	-2,99 V	
		=	int an	
	100,PA	3_01 V	-3,05 V	
	100.PA	2.96 V	-2,98 V	
	200,PA	2.94 V	+2,97 V	
A7 #300.PA 2	200.PA	2.94 V	-2.98 V	
CS1 =200.PA 3	SOO,PA	2.97 V	•2,98 V	
	100, PA	5.99 A	±2,98 V =2,98 V	
	100 PA	2.95 V	#2,95 V #2,95 V	
	PA PA	2.98 V	#2,96 V	
· · · · · · · · · · · · · · · · · · ·				
DIØ -300.PA 8	200 PA	3.03 V	-2,97 V -2,96 V -2,96 V	
DI1 #200.PA E	00.PA	3.02 V	+2.96 V	
-	00.PA	3.03 V	-2.96 V	
	200.PA	3.03 V	=2.97 V	
·	ew er wet oo	- · · · · · · · · · · · · · · · · · · ·	The state of the s	

RÇA	COP1882SD	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP:	-50 C	SNI	54
					PÄGE	4 OF	19	
	מסמ	100	למת	003		·		
VOL2 VOL2 VOH1	4,88 V	100,4V 105,4V 4,88 V 9,82 V	105.MV 120.MV 4,88 V 9.81 V	105,4V 120,4V 4,88 V 9,82 V				
IDN1 IDN2 IDP1 IDP2	-3.17MA	7'.45MA 17.8MA -3.17MA -6.82MA	7.05MA 15.8MA ~3.11MA ~6.55MA	7' 05MA 16 0MA -3,13MA -6,82MA				
1071 1072 1073 1074	2.40NA 5.70NA	1,40NA 4,40NA 1,80NA -300,PA	5.10NA 1.70NA 3.50NA 7.00NA	700'PA 3'70NA 2'90NA 4100'PA		·		
1025 1026 1027 1028	1.20NA 1.20NA	7,10NA 6,80NA 7,00NA 6,80NA	#200.PA #200.PA #200.PA	6,00NA 6,30NA 6,10NA 6.20NA				
ILDP	2,00UA							
IL1 IL2 IL3 IL4	-25.01A -35.0UA -75.0UA							

RCA	CDP1822SO	256 X 4	CMOS STATIC RAM	31 AUG 78	TEMP:	#55 C	SNI	54
	0				2102	E 65 (

PASSED	GALPAT	(MIDE	LIMITS)	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS)	V¢C≃5V

	VCC	= 4.5V	5.øv	10.0V
ADDRESS ACCESS TIME	(TAA)	230 N	180 N	70.0N
DATA SETUP TIME DATA HOLD TIME	(TDS) (TDH)	24,0N 10.0N	18,0N 10,0N	6.00N 14.0N
	-	10.0N	8	•
ADDRESS SETUP TIME ADDRESS SETUP TIME	(TAS1) (TAS2)	110.N	88.0N ,	4.00N 36.0N
ADDRESS HOLD TIME WRITE PULSE WIDTH	(HAY) (9WT)	⊷14,0N 72.0N	+12.0N 60.0N	-2.00N NO.0E
CS1 SETUP TIME CS2 SETUP TIME	(TCSS1) (TCSS2)	136 N 136 N	118 N 116 N	56,0N 54,0N
CS1 HOLD TIME	(TCSH1)	42.0N	30, an	20,0N
CS2 HOLD TIME	(TCSH2)	46'. ØN	34.0N	18 2N
OUTPUT ACTIVE FROM CS		226.N	176°N	80,0N
OUTPUT ACTIVE FROM CS		224.N 40.0N	174.N 36.0N	78,0N 22.0N
•				
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM CS2	(11400T) (SHOOT)	130 N 128 N	100'N 98.00	35,0N
OUTPUT HOLD FROM MRD	(TDOH3)	134.N	112,N	28,0%
OUTPUT HOLD FROM MWR	(TPNH)	130 N	108,N	28, ØN
READ CYCLE TIME WRITE CYCLE TIME	(TRC) (TWC)	216.N 200.N	184 ₂ N 168.N	88,0N 96.0N
IIL	ІІН	Aici	vtca	
A0 0,00 A	0 0 A O A	3.12 V	-3-08 V	
A1 =100.PA	100 PA	3.12 V	-3,14 V	
A2 #100.PA A3 0.00 A	100 PA 100 PA	3.12 V 3.10 V	-3,14 V -3,18 V	
	4 m m ' m 4	9		
A4 0.00 A A5 0.00 A	100,PA 100,PA	3,13 V 3,08 V	=3,16 V =3,10 V	
A6 #100.PA	100,PA	3,06 V	-3.09 V -3.10 V	
A7 =100.PA	100.PA	3.06 V		
CS1 =100.PA	100, PA	3.09 V	-3,10 V	
CS2 =100.PA MWR =100.PA	100.PA 0.00 A	3,11 V 3,08 V	-3,10 V -3,08 V	
MRD =100.P4	100.PA	3.10 V	-3.08 V	
DI0 -100.PA	100 PA	3,14 V	-3.09 V	
DI1 0.00 A	100.PA	3,14 V	-3,09 V	
DI2 =100.PA DI3 =100.PA	0.00 A 100.PA	3,15 V 3,15 V	#3,08 V -3,09 V	
rea republic	e u w p i m	~ # T ™ A		

RÇA	CDP1822SD	256 X 4	CMOS STATIC RAM	31 AUG 78	TEMP:	⇒ 55 C	SN:	24
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	DOØ	001	500	003
VOL 4	DE AMU	og gwy	95,0MV	OR AUG
VOL 1	85,0MV	90.0MV		95.0MV
AOLS	85.0MV	95.0MV	105.HV	105.MV 4,89 V
VOH1	4 89 V	4 89 V	4.89 V	4,89 V
AOHS	9.84 V	9,84 V	9.84 V	9,85 V
IDN1	8.65MA	8,25MA	7.80MA	7 BOMA
IDNZ	21.7MA	19,8MA	17.8MA	18.0MA
IDP1	-3.60MA	-3,65MA	-3.61MA	#3,63MA
IDPS	-7.76MA	-7.86MA	-7.59MA	-7.84MA
THEE	-1 * LDIAW	→ f • O O Pri M	कर⊞ झाउलाक्ष	# (# Dana
IOZ1	6.10NA	-1.80NA	5.30NA	-1.50NA
ioza	2.90NA	-300.PA	3.00NA	-700.PA
IUZ3	-100 PA	2 80NA	#800.PA	3.90NA
	-	-500 PA	2.70NA	600.PA
1024	4.00NA	# DWM B PA	E N I WINA	DUDETA
1025	200.PA	8,60NA	600.PA	1 40NA
1026	400 PA	2.10NA	600.PA	1,60NA
1027	400 PA	2.40NA	800 PA	1,20NA
	-			
1028	600.PA	1.80NA	900 . PA	1,40NA
ILDP	-200.NA			
71.4	25 4114			
ILI	-25,0UA			
ILS	≖35.0UA			
IL3	≈75.0UA			
IL4	⊶75,0UA			

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PASSED	GALPAT	(WIDE	LIMITS)	VCC=10V	
			LIMITS) LIMITS)	VCC≠10V VCC=5V	REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

	vcc	= 4.5V	5 . 0v	10'.0V
ADDRESS ACCESS TIME	(TAA)	240 N	205'N	90, an
DATA SETUP TIME	(TDS)	18,0N	16.0N	8.00N
DATA HOLD TIME	(100)	18.0N	16.0N	18.9N
DATA OBED 1100	(turi j	10.004		1082
ADDRESS SETUP TIME	(TAS1)	6,00N	6.00N	4.00N
ADDRESS SETUP TIME	(TASE)	120 N	98.0N	50,0N
ADDRESS HOLD TIME	(HAT)	-16.0N	-14 , MN	⇒ ନ୍ଦ୍ରଧ
WRITE PULSE WIOTH	(TWP)	72.0N	64 # MN	38,0N
CS1 SETUP TIME	(TCSS1)	158.N	140 N	72 ° 0N
CS2 SETUP TIME	(TCSS2)		136 N	
		156.N		72,0N
	(TCSH1)	44,0N	40.0N 42.0N	56,0N 56,0N
CSS HOLD TIME	(TCSH2)	48 @N	4 C . WIV	
OUTPUT ACTIVE FROM CS1	(TDOA1)	236.N	500,N	98 ู้ ตก
OUTPUT ACTIVE FROM CS2	(TDOA2)	234.N	198.N	98, ØN
OUTPUT ACTIVE FROM MRD	(TDOA3)	52.0N	46 . ON	28 0N
DUTCHT HOLD COOM AC.	CTDDWis	4 // Q hi	116.N	38, ØN
OUTPUT HOLD FROM CS1	(TDOH1)	148.N		
OUTPUT HOLD FROM CS2	(TD6H2)	144,N	114,N	38,0M
OUTPUT HOLD FROM MRD	(TDOH3)	140 N	118,N	34 ØN
OUTPUT HOLD FROM MWR	(TPDH)	136.N	114,N	32 0N
READ CYCLE TIME	(TRC)	264.N	224,N	112.N
WRITE CYCLE TIME	(TWC)	208.N	184.N	128.N
IIL I	Hľ	VICI	A1C5	
AØ +14,8NA 1	7.1NA	2.76 V	<u>+</u> 2,73 V	
	8.0NA	2.77 V	a Bø v	
r · · · · · · · · · · · · · · · · · · ·	7.7NA	2.76 V	-2 80 V	
*	8.2NA	2.73 V	-2.76 V	
A4 -14,8NA 1	19.3NA	2.78 V	-2,83 V	
A5 =15,3NA 1	8,7NA	2.72 V	÷2,75 V	
	20.5NA	2.70 V	-2.73 V	
A7 =16.0NA 2	21.7NA	2.70 V	-2.75 V	
CS1 +16,0NA 8	22.2NA	2.73 V	-2,74 V	
	22.7NA	2.75 V		
■	7.6NA	2.72 V	-2,76 V -2,72 V	
• •	9.4NA	2.74 V	==,73 V	
	, ramely 94	C: b f '99 V		
	7,4NA	2.79 V	-2.74 V	
DI1 ≈18,8NA ã	27.2NA	2.78 V	+2,73 V	
	27.1NA	2.80 V	#2,73 V	
DI3 -21.0NA 2	28.2NA	2.79 V	-2.75 V	
-		T 605		

RCA	COP182250	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP	85 C	SNI	24
	•				PÄGE	8 OF	10	
	DOØ	001	500	003				
VOL1 VOH1 VOH2	125.MV 135.MV 4.82 V 9.74 V	135,MV 150,MV 4,82 V 9,74 V	145.MV 170.MV 4.82 V 9.73 V	140'MV 165'MV 4'82 V 9'74 V				
IDN1 IDN1 IDP1 IDP2	5.85MA 14.2MA =2.23MA =4.81MA	5,55MA 12,8MA -2,20MA -4,80MA	5.25MA 11.3MA =2.18MA =4.64MA	5,25MA 11,6MA -2,21MA -4.81MA				
1021 1022 1023 1024	235.NA 235.NA 236.NA 225.NA	211,NA 208,NA 205,NA 209,NA	235, NA 226, NA 228, NA 220, NA	221, NA 225, NA 221, NA 227, NA				
1025 1026 1027 1028	230.NA 225.NA 225.NA	210,NA 220,NA AN, 205 AN, 215	228 NA 224 NA 233 NA 222 NA	228, NA 222, NA 217, NA 227, NA				
14.DP	9,00UA							
161 262 163 164	=45,0UA =65.0UA ⇔100.UA ∞100.UA							

PASSED GALPAT (WIDE LIMITS) VCC=10V PASSED GALPAT (TIGHT LIMITS) VCC=10V PASSED GALPAT (TIGHT LIMITS) VCC=5V

	vcc	ж 4 _ж 5ү	5. ØV	10.0V
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA) (TDS) (TDH)	255.N 20.0N 20.0N	20.0N 16.0N 220.N	100 N 8 400N 20 10N
ADDRESS SETUP TIME ADDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WIDTH	(TAS1) (TAS2) (TAH) (TWP)	4,00N 128.N +18.UN 78.0N	4.00N 106.N -14.0N 70.0N	4.00N 58.0N -2.00N 42.0N
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS1) (TCSS2) (TCSH1) (TCSH2)	172,N 168.N 46,0N 50.0N	150, N 148, N 42, ON 46, ON	80,0N 78,0N 28,0N 28,0N
OUTPUT ACTIVE FROM CS: OUTPUT ACTIVE FROM MRD	(SACOT)	258 N 256 N 56 ON	220',N 218',N 50', 0N	/ 110.N 106.N 30.0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH1) (TDOH2) (TDOH3) (TPOH) (TRC) (TWC)	152 N 148 N 140 N 140 N 288 N 216 N	122, N 118, N 120, N 116, N 240, N 200, N	42,0N 42,0N 36,0N 38,0N 128,N 136,N
TIL	ITH	VICI	AICS	
A1 =91,8NA 9	90.6NA 91.4NA 92.1NA 90.7NA	2.68 V 2.69 V 2.66 V	-2,65 V -2,73 V -2,72 V -2,69 V	
45 =90,3NA 9	94.9NA 93.3NA 94.5NA 98.8NA	2.71 V 2.64 V 2.63 V 2.63 V	=2,75 V =2,67 V =2,67 V =2.67 V	
CS2 #99,9NA 1	97.4NA 101.NA 90.5NA 91.8NA	2.65 V 2.67 V 2.64 V 2.66 V	72,67 V 72,69 V 72,64 V 72,66 V	
DI1 =94.9NA 1	104, NA 103, NA 103, NA 106, NA	2.72 V 2.71 V 2.72 V 2.72 V	72,66 V 72,66 V 72,66 V 72,67 V	

RCA	CDP1822SD	256 X 4 CMOS	STATIC RAM	38 AUG 78	TEMP:	125 C 5Ni
					PAGE	10 OF 10
	poø	poi	200	003		
AOP5 AOP5 AOP7	140 MV 150 MV 4 80 V 9 71 V	150' MV 165 MV 4,80 V 9,71 V	160.MV 190.MV 4.80 V 9.70 V	160,MV 155,MV 4,80 V 9,70 V		
IDN1 IDN2 IDP1 IDP2	5.25MA 12.7MA -2.00MA -4.31MA	4'.95MA 11.4MA -2.00MA -4.33MA	4_70MA 10_1MA =1_96MA =4_16MA	4,70MA 10,3MA 1,99MA 44.30MA		
1021 1022 1023 1024	9492NA 9364NA 927.NA 925.NA	915,NA 899.NA 901.NA 888.NA	973,NA 974.NA 967.NA 967.NA	AN,550 AN,650 AN,650 AN.550		
1025 1026 1027 1028	936.NA 946.NA 932.NA 934.NA	905,NA 906,NA 910,NA 895.NA	989.NA 974.NA 972.NA 975.NA	948,NA 947,NA 937,NA 932.NA		٠,
ĭLDP	40 QUA					
IL1 IL2 IL3 IL4	-105.UA -145.UA -180.UA -165.UA					

PAGE 1 OF 10

			rat	3C 1 UT 10
PASSED GALPAT (WIDE	LIMITS) VO	C=10V	REPRODUCIB:	ILITY OF THE
		C=10V	ORIGINAL PA	GE IS POOR
PASSED GALPAT (TIGH	T LIMITS) VO	:C#5V		
FAILED DATA RETENTION	N TEST ADD =	51 DIAG s	34 PIN: 0	302
	VCC	= 4.5V	5'. ØV	10.00
ADDRESS ACCESS TIME	(TAA)	21Ø.N	180'N	75,0N
DATA SETUP TIME	(TDS)	22, ØN	18.0N	8.000
DATA HOLD TIME	(TDH)	10,0N	19.0N	12.0N
AUDRESS SETUP TIME	(TAS1)	10.0N	8.00N	4.001
ADDRESS SETUP TIME	(TAS2)	102.N	88.00	42.0N
AUDRESS HOLD TIME	(HAT)	-14,0N	-10.0N	-5.00N
WRITE PULSE WIDTH	(TWP)	65. QN	54.0N	32.0N
CS1 SETUP TIME	(TCSS1)	146.N	126, N	62, ØN
CS2 SETUP TIME	(TCSS2)	142.N	122.N	60,0N
CS1 HOLD TIME	(TCSH1)	40,0N	36.0N	24,0N
CS2 HOLD TIME	(TCSH2)	42.ØN	38.0N	55.0N
DUTPUT ACTIVE FROM C	S1 (TDOA1)	202,0	174, N	82,0N
OUTPHT ACTIVE FROM C		200.N	170 N	82, ØN
OUTPUT ACTIVE FROM MI		46.0N	40.0N	24.0N
OUTPUT HOLD FROM CS1	(TOOH1)	138,N	198°N	79 GN
OUTPUT HOLD FROM CS2	(SHOUT)	134.N	1906 N	32.0N
OUTPUT HOLD FROM MRD	(TOOH3)	136.N	106 N 114 N	PR ON
OUTPUT HOLD FROM HWR	(TPDH)	130.N	110 N	30,0N 30,0N 96,0N
READ CYCLE TIME	(TRC)	224.N	500 N	96 ØN
WRITE CYCLE TIME	(TWC)	224.N	176.N	104.N
ItL	II#	VIC1	vtca	
A0 =2.00NA	ສ່ດຄະ.	5 5 4 11	- ,	
A1 =2,60NA	3.90NA 2.20NA	2.94 V 2.97 V	-2,93 V	
A2 -2.10NA	1,90NA		=2,99 V	
A3 -1.90NA	2.00NA	2.99 V	-3.00 V -3.00 V	
A4 =2.10NA	1.80NA	7 03 V	-3,02 V	
A4 =2.10NA A5 =2.30NA	2.00NA	3,02 V 2.91 V	-3.02 V	
A6 -2.00NA	2.10NA	2.88 V	2,93 V 2,91 V	
A7 -2.20NA	2.10NA	2.89 V	-5. 35 A	
CS1 =2,20NA	1.80NA			
CS2 =2,70NA	2,20NA		=2,95 V =3 00 V	
MWR -2.60NA	2.20NA		⊕3,00 V ⊕2,95 V	
MRD -1.90NA	2.40NA	2.94 V	-2.94 V	
010 -2.50NA	1.90NA	2.97 V	-2,94 V	•
DI1 =1.80NA	2.90NA	2.96 V	e2,91 V	
DIS ~2.20NA	2,10NA		-2,94 V	
DI3 -2.50NA	1.80NA		#2.94 V	
.			- -	

RCA	CDP1822SD	256 X 4 CMDS	STATIC RAM	31 AUG 78	TEMP	25 C	sn:	25
					PAGE	2 OF	10	
	non	D01	500	003				
VOLI	9ฅ ู้ ผูพ v	95.0MV	105.MV	105, HV				
VOL2	95.0MV	110.MV	130 MV	125.MV				
VUH1	4.86 V	4,86 V	4.86 V	4,86 V				
VUHŽ	9.80 V	9.80 V	9.80 V	9 80 V				
TON1	8,15MA	7.60MA	6.90MA	7.05MA				
IDMS	19.6MA	17.4MA	14.9MA	15.5MA				
IDPi	₩2,83MA	-2.81MA	-2.71MA	-2,83MA				
IDP2	-6.26 MA	-6.23MA	-5.94MA	#6.31MA				
IOZI	34.0NA	39,1NA	33,1NA	36.184				
IUZZ	36.7NA	35,0NA	36.6NA	32,6NA				
1023	33.1NA	37.9NA	35 1NA	32.BNA				
1024	31.4NA	40.6NA	32.4NA	36.4NA			٠	
1025	38,5NA	33,6NA	39 2NA	31,3NA				
1076	38.8NA	34.4NA	39.5NA	30.9NA				
1027	38,8NA	34,3NA	38,9NA	30,8NA				
IOZ8	38.684	34,2NA	39 . UNA	30.7NA				
71 54.77	10 0114							
ILDP	-10.0UA							
ILS	-160.UA							
ILS	-18Ø _a UA							
IL3	-25,0UA							
IL4	-40.ØUA							

PAGE 3 OF 10

	IT LIMITS) VC	C=10V C=10V C=5V	REPRODUCIBILITY ORIGINAL PAGE	
FAILED DATA RETENTIO	N TEST ADD =	51 DIAG	≈ 34 PIN: 00	2
	vcc	≖ 4.5V	5 . Ø V	10.0V
AUDRESS ACCESS TIME	(TAA)	aam,N	180'N	70.0H
DATA SETUP TIME	(TOS)	24 ØN	18.0N	6.00N
DATA HOLD TIME	(אמד)	8.00N	8.00N	10.0N
ADDRESS SETUP TIME	(TAS1)	16.0N	18.00	4.000
ADDRESS SETUP TIME	(TAS2)	104.N	84. AN	38,ØN
ADDRESS HOLD TIME	(TAH)	-12.0N	-10.0N	-5.00N
WRITE PULSE WINTH	(TWP)	60.0N	52. 9N	32,0N
CS: SETUP TIME	(TCSS1)	144 . N	120,N	58. ØN
CS2 SETUP TIME	(TCSS2)	(42 N	118 N	56,0N
CS1 HOLD TIME	(TCSH1)	36, ØN	32,0N	55, 0N
CS2 HOLD TIME	(TCSH2)	38.0N	35.0V	20.04
OUTPUT ACTIVE FROM C	S1 (TOOA1)	206.N	168,N	80,0N
OUTPUT ACTIVE FROM C	(SAOOT) SE	204.N	166.N	78, ØN
QUTPUT ACTIVE FROM N	IRD (TDOA3)	42.0N	38 , ØN	25.0N
OUTPUT HOLD FROM CS:	(TDOH1)	132.N	104, N 102, N 112, N 108, N	32,0N
OUTPUT HOLD FROM CSE	(SHOOT)	130 N	102,N	32,00
DUTPUT HOLD FROM MRO		134,N	112 N	P8,0N
DUTPUT HOLD FROM MWR		128.N	108,N	28,00
READ CYCLE TIME	(TRC)	216.N	195'V	88,00
WRITE CYCLE TIME	(TWC)	208 N	168.N	96'. ØN
IIL	IIH	AICI	AICS	
A0 -300.PA	1.10NA	3.03 V	-3,02 V	
A1 -600.PA	500,PA	3.96 V	-3 08 V	
A2 #300.PA	400,PA	3.10 V	-3,11 V	
A3 +300.PA	300.PA	3.19 V	-3.10 V	
A4 #400 PA	200.PA	3.11 V	-3,11 V	
A5 =400.PA	300,PA	3.01 V	-3,02 V	
A6 =400.PA	400.PA	2,97 V	-3,01 V	
A7 =500.PA	300.PA	2.99 V	-3.01 V	
CS1 =400.PA	300.PA	3.04 V	-3,04 V	
CS2 +500.PA	800.PA	3.06 V	+3,09 V	
MWR #500_PA	400,PA	3.04 V	-3,03 V	
MRO #300.PA	500.PA	3.03 V	∞3.03 V	
DI0 -500.PA	300.PA	3'.07 V	#3,03 V	
DI1 +300 PA	700,PA	3.06 V	-3,01 V -3,03 V	
DI2 -500,PA	400 PA	3.08 V	-3,03 V	
013 -500 PA	300.PA	3.05 V	-3.03 V	

RCA	COPIBERSO	256 X 4	CMOS STATIC	RAM ~31	AUG 78	TEMP:	#50 C	SN:	25
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PAGE 4 0F 10

	שמם	100	200	003
VOH2	80.0MV	85.0MV	95'.ØMV	90 MMV
	85.0MV	95.0MV	110.MV	105 MV
	4.88 V	4.88 V	4.88 V	4,88 V
	9.84 V	9.84 V	9.83 V	9.84 V
IDN1	9.10MA	8.50MA	7.80MA	7.95MA
IDN2	22.3MA	19.9MA	17.2MA	17.8MA
IDP1	-3.30MA	-3.33MA	-3.22MA	27.30MA
IDP2	-7.31M4	-7.35M4	-7.01MA	27.30MA
1021	7.10NA	4,80NA	5.30NA	4,90NA
1022	9.00NA	2,10NA	9.00NA	1,70NA
1023	1.70NA	9,20NA	2.00NA	8,10NA
1024	3.00NA	7.50NA	2.50NA	7,40NA
1025	7.40NA	2.60NA	ANDS.8	1,49NA
1026	7.60NA	2.50NA	ANDS.8	1,49NA
1027	7.50NA	2.50NA	ANDS.8	1,29NA
1028	7.60NA	2.20NA	ANDS.8	1,49NA
ILDP	-2.80UA			
IL1 IL2 IL3 IL4	-165.UA -180.UA -20,0UA -35.0UA			

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PASSED GALPAT (WIDE LIMITS) VCC=10V PASSED GALPAT (TIGHT LIMITS) VCC=10V PASSED GALPAT (TIGHT LIMITS) VCC=5V

	, +++, +, +, A.C.	4, 1		
FAILED DATA RETENTION	N TEST ADD *	51 DTAG	= 34 PINI	808
	vcc	= 4.5V	5 <u>.</u> 0v	10.0V
ADDRESS ACCESS TIME	(TAA)	220 N	175'N	65'.ØN
DATA SETUP TIME	(TDS)	32. ØN	55 WN	6.00N
DATA HOLD TIME	(TOH)	6.00N	8.000	10.0N
ADDRESS SETUP TIME	(TAS1)	14.0N	10,9N	4.70N
ADDRESS SETUP TIME	(TASE)	100.N	85 01	34 ON
ADDRESS HOLD TIME	(TAH)	-14,0N	-10.0N	-2.00N
WRITE PULSE WINTH	(TWP)	76.0N	52.0N	30.0N
CS1 SETUP TIME	(TCSS1)	142.N	188,0	5 4 ¹ 0 N
CS2 SETUP TIME	(TCSS2)	144 N	116.N	54,0N 54,0N
CS1 HOLD TIME	(TCSH1)	46, DN	34,0N	ag, an
CS2 HOLD TIME	(TCSH2)	46.0N	38.0N	20.0N
		20.00		
OUTPUT ACTIVE FROM C		208.N	166 N	78.0N
OUTPUT ACTIVE FROM C		206.N	162.N	76,0N
OUTPUT ACTIVE FROM MI	(EADOT) OF	40'. ON	34.7N	50 GN
OUTPUT HOLD FROM CS1	(TOOH1)	128.N	98.0N	30,0N
OUTPUT HOLD FROM CS2	(TOOH2)	126.N	96. AN	30 โตก
OUTPUT HOLD FROM MRD	(TDOH3)	134.N	112,N	26,0N
DUTPUT HOLD FROM MWR	(TPDH)	128.N	106,N	28,00
READ CYCLE TIME	(TRC)	216.N	184,N	
WRITE CYCLE TIME	(TWC)	216.N	160 N	88,0N 88,0N
IIL	IIH	VICt	VICR	
AØ -100.PA	4MD.PA	3.13 V	±3,11 V	
A1 +200.PA	100,PA	3.15 V	-3,17 V	
A2 -100.PA	100,PA	3.18 V	-3.20 V -3.18 V	
A3 =100,PA	100_PA	3.18 V	=3.18 V	
A4 -tan.PA	100.PA	3.20 V	-3,19 V	
A5 ~100.PA	100,PA	3,11 V	-3.12 V	
A6 -100.PA	100,PA	3.06 V	-3,11 V	
A7 =100.PA	100.PA	3.09 V	43 € 1 Ø V	
CS1 -100.PA	100 PA	3_13 V	-3,13 V	
CS2 -100 PA	200, PA	3,15 V	-3,18 V	
MWR =100 PA	100 PA	3,13 V	=3,13 V	
MRD -100.PA	100 PA	3.13 V	*3.12 V	
DIØ =100.PA	100.PA	3,16 V	-3,13 V	
DI1 -100 FA	200.PA	3.15 V	-3,10 V	
DI2 #200_PA	100 PA	3.17 V	-3,12 V	
DI3 =100.PA	100.PA	3.15 V	-3,13 V	

RCA	CDP182280	256 X 4	CMOS STATIC RAM	31 AUG 78	TEMP:	#55 C SN:	25
					2165	4 65 45	

	DOM	001	nos	D03:
VOL 1	75.0MV 75.0MV	80.0MV	85.0MV	85.0MV
VOLE VOH1	4.90 V	85,0MV	100.MV	95.0HV
AOUT	9.85 V	4,90 V 9.86 V	4.90 V 9.85 V	4,90 V 9,85 V
₹UI1E	a € tra A	7.00 V	7 4 CO 4	V הסביל V
IDN1	9.95MA	9,35MA	8.55MA	8 .7 0MA
IDNS	24.7MA	22.2MA	19.3MA	19.9MA
IDP1	-3.79MA	-3,80MA	-3.73MA	-3 A3MA
IDP2	-8.35MA	-8.41MA	-8.06MA	-8.50MA
	•			- . .
IOZI	700.PA	3,60NA	1.00NA	2,00NA
IOZZ	-1.20NA	5,70NA	-1.70NA	5,50NA
1023	5.70NA	-2.00NA	5.50NA	-1.60NA
IDZ4	2.70NA	300.PA	3.20NA	-400 PA
1025	600.PA	3,30NA	-400.PA	4,00NA
1076	1.00NA	3,30NA	-500.PA	3,70NA
1027	900.PA	3,00NA	-100.PA	3,70NA
1028	1.30NA	2.90NA	~200.PA	3,40NA
91.00	5 5 0114			
ILDP	-20,0UA			
ILI	-175,UA			
ĭĽŝ	-190 UA			
ÎL3	=15.0UA			
IL4	-30.0UA			
	~ 가장 B 안녕된			

			P	AGE 7 OF 1
PASSED GALPAT (TIGH	T LIMITS) VC	C=10V C=10V C=5V	reproducibili original page	
FAILED DATA RETENTIO	N TEST ADD =	51 DIAG	= 34 PINI	992
	vcc	= 4.5V	5'.øv	10.00
ADDRESS ACCESS TIME	(TAA)	205.N	180 N	80.01
DATA SETUP TIME	(TDS)	55,0N	18,0N	8 . 90N
DATA HOLD TIME	(TDH)	12.0N	12.0N	12.00
ADDRESS SETUP TIME	(TAS1)	8 . 00N	8. AAN	4.00N
ADDRESS SETUP TIME	(SZAT)	106 N	94,0N	48.0N
ADDRESS HOLD TIME	(TAH)	-12,0N	#10.0N	-5° Ğ Ø Ŋ
WRITE PULSE WINTH	(TWP)	72.ØN	64.7N	38.0N
CS1 SETHP TIME	(TCSS1)	150.N	128 N	66,0N
CS2 SETUP TIME	(TCSS2)	146.N	126.N	64, ØN
CS1 HOLD TIME	(TCSH1)	46, ON	42 " WN	26,0N
CS2 HOLD TIME	(TCSH2)	50.0N	aa.an	26.0N
DUTPUT ACTIVE FROM C	\$1 (TD0A1)	206.N	180'N	90,0N
	(SAOOT) SE	202.N	178.N	90,00
OUTPUT ACTIVE FROM ME	RD (TDOA3)	48.0N	42.0N	26_@N
OUTPUT HOLD FROM CS1	(TDOH1)	140,N	110 N	34,0N
OUTPUT HOLD FROM CS2	(TDOH2)	136.N	108 N	34,0N
OUTPUT HOLD FROM MRD	(TDOH3)	136.N	114 N	30, 0N
QUTPUT HOLD FROM MWR	(1004)	132.N	110,N	30.00
READ CYCLE TIME	(TRC)	535 N	500°V	112.N
WRITE CYCLE TIME	(TWC)	200.N	176.N	112.1
IIL	ITH	VIC1	\$21V	
A0 -22,0NA	28,9NA	2.91 V	-2,90 V	
A1 -24.0NA	ANB.SS	2.95 V	-2,97 V -3,00 V -2,94 V	
A2 -22,6NA	22.3NA	2.97 V	-3,00 V	
A3 =21.8NA	AN8.58	2.96 V	-2.9A V	
A4 =23,0NA	21.7NA	2.99 V	-3,00 V	
A5 -23,4NA	22.1NA	2.89 V	-2.91 V	
A6 #21,6NA	22.3NA	2.86 V	-2_89 v -2_89 v	
A7 -21.6NA	21.8NA	2.87 V	-2.89 V	
CSI =24.1NA	20.8NA	5.95 A	-2,93 V	
C\$2 #22,7NA	22,6NA	2.94 V	<u>-</u> 2,98 V	
MWR -23,4NA MRD -21.8NA	22.6NA	2.92 V	₩2,93 V	
MRD =21.8NA	23.2NA	2.91 V	=2,92 V	
DI0 -22.2NA	21.1NA	2.95 V	#2,91 V	
0I1 -20,1NA	23.6NA	2,94 V	-2,89 V	
DI2 -20,5NA	21.2NA	2.96 V	91 ۷ و چې	
DI3 =20.6NA	20.1NA	2.94 V	#2.92 V	

RCA	CDP18225D	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP:	85 C SN:
					PAGE	8 OF 10
	DOB	001	500	p03		
VOLi	105.MV	110,MV	125.MV	120.MV		
AQF5	115.MV	130 MV	150.MV	145.MV		
VOM1	4.84 V	4,84 V	4.84 V	4,84 V		
ANHS	9.77 V	9.77 V	9.76 V	9.77 V		
IDNI	7.10MA	6.60MA	6.90MA	6.15MA		
IDMS	16.8MA	14.9MA	12.7MA	13.3MA		
IDP1	-2.40MA	-2,37MA	-2.33MA	#2,41MA		
INPS	-5.31MA	AMDE.E-	⇒5.Ø6MA	=5,37MA		
1021	316 .NA	305 NA	305.NA	280°,NA		
Ioza	318.NA	30 3 ,NA	300 NA	287, NA		
1023	314.NA	302,NA	303.NA	283,NA		
IOZ4	316.NA	304.NA	298 NA	292 NA		•
1025	319,NA	306, NA	306.NA	297 NA		
1026	314,NA	321,NA	298.NA	292,NA		
1027	312.NA	309,NA	308_NA	284 NA		
IUZ8	318,NA	308.NA	300.NA	294.NA		
ILDP	3.00HA					
IL1	≈180,UA ≈200.UA					•
1L3 1L4	⇔45,0UA -55.0UA					

PAGE 9 0F 10

PASSED	GALPAT	(WIDE	LIMITSI	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS)	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS	VCC=5V

\$1,441,	,,	5.		
FAILED DATA RETENTION	N TEST ADD =	51 DIAG	= 34 PİN:	aas
	vcc	≈ 4.5V	5.0V	10,00
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA) (TDS) (TDH)	215.N 22.ØN 14.ØN	190.N 18.0N 14.0N	90,0N 8,00N 14,0N
ADDRESS SETUP TIME ADDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WIDTH	(TAS1) (TAS2) (TAH) (TWP)	6.00N 114.N -12.0N 76.0N	4 09N 102 N -10 0N 68 0N	4.00N 54.00N -2.00N 40.0N
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS1) (TCSS2) (TCSH1) (TCSH2)	152.N 150.N 48,0N 52.0N	134 N 132 N 44 M 46 M	70,0N 70,0N 28,0N 28,0N
OUTPUT ACTIVE FROM COUTPUT ACTIVE FROM ME	(SADOT) SE	216.N 214.N 50.0N	192, N 188. N 44. MN	102.N 98,0N 88.0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH1) (TDOH2) (TDOH3) (TPDH) (TRC) (TWC)	140.N 138.N 136.N 132.N 232.N 208.N	112'N 108'N 116'N 116'N 208'N	36,0N 34,0N 30,0N 32.0N 112.N 120.N
III.	IIH	VICI	VICE	
A0 =131.NA A1 =135.NA A2 =131.NA A3 =129.NA	138,NA 130,NA 128,NA 127.NA	2.89 V 2.93 V 2.96 V 2.95 V	=2,89 V =2,95 V =2,98 V =2.97 V	
A4 =130,NA A5 =130,NA A6 =126,NA A7 =123,NA	124, NA 122, NA 122, NA 122, NA	2,98 V 2.88 V 2,84 V 2.85 V	-2.99 V -2.89 V -2.87 V -2.88 V	
CS1 =133.NA CS2 =127.NA MWR =129.NA MRD =126.NA	118,NA 124,NA 123,NA 123,NA	2.91 V 2.93 V 2.91 V 2.89 V	=2,91 V =2,96 V =2,98 V	
DI0 -120.NA DI1 -115.NA DI2 -117.NA DI3 -115.NA	119.NA 119.NA 116.NA 114.NA	2.93 V 2.92 V 2.94 V 2.92 V	e2,89 V e2,88 V e2,90 V e2,91 V	

NUA	rot forest	E36 X 4 CML	O STATE RAN	31 AUG 78 TEMPI	10 OF		23
	מסמ	100	boà	003	• (* **)	•	
1401.4	4 4 27 1617	ADE! NU	á 11 m 1414	4 vm au * 1			

... :

	204		9 4 6	404
A0H5	115.MV	125 MV	140.MV	135, MV
A0H1	125,MV	145 MV	170.MV	160, MV
A0F5	4.82 V	4 82 V	4.81 V	4, 82 V
A0F1	9.74 V	9 73 V	9.72 V	9,74 V
IDM1	6.35MA	5.95MA	5.40MA	5,55MA
	15.0MA	13.3MA	11.4MA	11,9MA
	-2.18MA	-2.16MA	=2.08MA	+2,19MA
	-4.79MA	-4.77MA	=4.53MA	+4,86MA
1021	1.28UA	1,25UA	1.19UA	1,14UA
1022	1.28UA	1,23UA	1.20UA	1,13UA
1023	1.26UA	1,24UA	1.18UA	1,14UA
1024	1.27UA	1,22UA	1.20UA	1,13UA
1025	1.27UA	1,26UA	1.21UA	1,18UA
1026	1.27UA	1,26UA	1.20UA	1,15UA
1027	1.27UA	1,24UA	1.20UA	1,14UA
1028	1.28UA	1,24UA	1.21UA	1,14UA
ILDP	20.0UA			

ILDP 20.0UA
IL1 ~250.UA
IL2 ~285.UA
IL3 ~115.UA
IL4 ~120.UA

RCA	CD6185580	256 X 4	CMOS	STATIC R	RAM 3	L AUG	78	TEMP:	25	C	SN:	26

PAGE 1 OF 10

	(WIDE LIMITS)	
· ·	(TIGHT LIMITS) (TIGHT LIMITS)	 REPRODUCIBILITY OF THE
Dicera miti am	Telipeal Teas	ORIGINAL PAGE IS POOR

PASSED DATA RETENTION	J TEST		•	
	vcc	= 4.5V	5.0V	10'.0V
ADDRESS ACCESS TIME	(TAA)	245.N	205.N	85'.0N
DATA SETUP TIME	(TDS)	ลด ตก	16.0N	P. PON
DATA HOLD TIME	(TDH)	12.0N	12.0N	12.00
	***************************************		4 14 # ****	2 G # 44***
ADDRESS SETUP TIME	(YAS1)	12.0N	10.0N	4.00%
ADDRESS SETUP TIME	(TAS2)	116.N	96.0N	48 ON
ADDRESS HOLD TIME	(TAH)	-18,0N	-14,0N	=4.00N
WRITE PULSE WINTH	(TWP)	64.ON	60.0N	36.0N
			•	•
CSI SETUP TIME	(TCSS1)	154.N	134 N	68, ØN
CS2 SETUP TIME	(TCSS2)	150 N	132'.N	66,0N
CS1 HOLD TIME	(TCSH1)	36,0N	32.9N	55,0N
CS2 HOLD TIME	(TCSH2)	38.0N	34.0N	55.0N
AUTHUT LESSUE FOOL				
OUTPUT ACTIVE FROM CS		236 N	200, N	92, QN
OUTPUT ACTIVE FROM CS		234.N	198.N	90,0N
OUTPUT ACTIVE FROM ME	CEADOR)	52.0N	46. MN	28.0N
OUTPUT HOLD FROM CS1	(TDOH1)	142.N	112,N	42, ØN
DUTPUT HOLD FROM CS2	(TDOH2)	140.N	1 1 E p 19	
OUTPUT HOLD FROM MED	(TD0H3)	136.N	110 N 116 N	40,6N
OUTPUT HOLD FROM MWR	(TPDH)	132,0		28, ØN
READ CYCLE TIME	(TRC)	256,N	110, N	28.0N 120.N
WRITE CYCLE TIME	(TWC)	296 N	216.N 184.N	112.N
all a fac of or a CT, a	(ING)	E 711 g 14	104 TA	11554
TIL	ITH	VICI	Alcs	
A0 -1.50NA	1.40NA	2.80 V	-2,80 V	
A1 -2.00NA	1.30NA	2.84 V	-2,84 V	
A2 =1.30NA	1.60NA	2.85 V	-2,89 V	
A3 ~1.40NA	1.20NA	2.86 V	-2.87 V	
· · · · · · · · · · · · · · · · · · ·		. •		
A4 -1.20NA	1,70NA	2,84 V	-2,86 V	
A5 =1.40NA	1.30NA	2.79 V	≈2,81 V	
A6 -1.5@NA	1.60NA	2.80 V	~2,82 V	
A7 -1.50NA	1.30NA	5.81 A	-2,82 V -2,85 V	
624 4 664		.		
CS1 -1.40NA	1,80NA	2.84 V	-2,84 V	
CS2 -1.60NA	1,60NA	2.86 V	-2,88 V	
MWR -2,00NA	1,50NA	2.81 V	÷5,85 V	
MRD #1.80NA	1.70NA	2.82 V	-2.84 V	
010 -1.50NA	1.40NA	2,89 V	-2,84 V	
DI1 -1.30NA	1,7004	2.89 V	#2,83 V	
DIS -2.00NA	1.50NA	ล์ 89 V	-2,84 V	
DI3 -1.70NA	2.00NA	2.87 V	-2.83 V	
= # 1 = 1 1				

RCA	COPIBEESO	256 X 4 CMDs	STATIC RAM	31 AUG 78	TEMP:	25 C	ŞN:	26
					PAGE	2 OF	10	
	nnø	001	pae	003				
AOH5 AOH1 AOF5 AOF1	110.MV 120.MV 4.84 V 9.70 V	115,MV 145.MV 4,84 V 9,69 V	130 MV 170 MV 4 84 V 9 68 V	125, MV 175, MV 4,84 V 9,69 V				
IDN1 IDN2 IDP1 IDP2	6.60MA 16.3MA =2.49MA =4.64MA	6.30MA 14.6MA ~2.57MA ~4.68MA	5_90MA 12_6MA -2_49MA -4_48MA	6,00MA 12,9MA =2,53MA =4,66MA				
1021 1022 1023 1024	12.8NA 15.6NA 9.00NA 8.50NA	10.6NA 6.80NA 11.5NA 12.4NA	8_50NA 12_0NA 7_70NA 6_30NA	11.6NA 8.20NA 11.6NA 13.9NA				
1025 1026 1027 1028	15.0NA 15.3NA 15.0NA 15.3NA	6,10NA 5,70NA 5,90NA 5,60NA	13,4NA 13,4NA 13,5NA 13.2NA	6.80NA 6.90NA 6.70NA				
ILDP	15.ØUA							
IL1 IL2 IL3 IL4	-9.05MA -9.02MA -10.2MA -10.2MA							

PAGE 3 OF 10

PASSED	GALPAT	(WIDE	LIMITS)	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS	VCC=5V

PASSED DATA RETENTION I	E91			
	VCC	= 4.5V	5. 0V	10'.0V
AUDRESS ACCESS TIME	CTAAT	ኃ/15 አ	200 ใ	75.0N
	(TAA)	245.N		
DATA SETUP TIME	(TDS)	22,0N	18.9N	8.000
DATA HOLD TIME	(HOT)	10.0N	10.0N	10.0N
ADDRESS SETUP TIME	(TAS1)	16.0N	12.ØN	4.00N
ADDRESS SETUP TIME	(TASE)	114.N	98.0N	42.0N
AUDRESS HOLD TIME	(TAH)	-16,ØN	-12.0N	-5.60M
WRITE PULSE WINTH	(TWP)	70.0N	58.AN	35.0N
WALLE FORSE WILLIAM	CIMED	I AS W AS IA	25 th ■ to its	>
CS1 SETUP TIME	(TCSSI)	148 N	158 N	62,0N
CS2 SETUP TIME	(TCSS2)	148 N	176 N	60,0N
CS1 HOLD TIME	(TCSH1)	34, ON	30.0N	az an
CS2 HOLD TIME	(TCSH2)	38.0N	32.00	20.00
, , , , ,	• • • • • • • • • • • • • • • • • • • •			
OUTPUT ACTIVE FROM CS1	(TDGA1)	236.N	192,N	86, ØN
OUTPUT ACTIVE FROM CS2	(SADOT)	234 N	192.N	84, ØN
OUTPUT ACTIVE FROM MRD	(TDOA3)	48 ÖN	42.AN	26. an
		_		
OUTPUT HOLD FROM CS1	(TDOH1)	136.N	106, N	38,0N
OUTPUT HOLD FROM CS2	(TDOH2)	134.N	104, N	38, ØN
OUTPUT HOLD FROM MRD	(TOOK3)	134.N	112 N	26,0N
OUTPUT HOLD FROM MWR	(TPOH)	132.N	106, N	28,0N
READ CYCLE TIME	(TRC)	838.N	500°N	96.04
WRITE CYCLE TIME	(TWC)	208.N	176 . N	124.N
IIC II	H	VICI	AICS	
AØ =200.PA 30	Ø.PA	2.95 V	-2,95 V -2,99 V -3,03 V	
_	Ø,PA	2.99 V	-2 99 V	
	0,PA	3.00 V	-3 03 V	
	Ø.PA	3.01 V	-3.01 V	
				
A4 -200.PA 30	0,PA	2.99 V	-3,00 V	
	Ø.PA	2.94 V	-2,97 V	
A6 =300.PA 30	Й _Р РА	2.95 V	-2,97 V	
	Ø.PA	2.96 V	-3,00 V	
			- +	
	0.PA	2.99 V	-2,98 V	
	Ø,PA	3.00 V	#3,02 V	
	Ø,PA	2.96 V	⊷2,97 V	
MRD =400.PA 40	Ø.PA	2.97 V	#2.98 V	
DIØ =300.PA 20	Ø.PA	3.03 V	-2,98 V	
	Ø _# PA	3.03 V	#2,97 V	
	Ø _a PA			
		3,03 V	-2,97 V	
DI3 =300 PA 40	0.PA	3.02 V	=2.97 V	

RCA	C0218228D	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP:	÷50 C	SNI	56
					PAGE	4 OF	10	
	DOM	001	pos	003				
VOL1	100,MV	105 MV	110.MV	110 MV				
ADF 5	105.MV	125.MV	145.MV	150 MV				
VOH1	4.87 V	4,87 V	4.86 V	150 MV 4 87 V				
SHOA	9,76 V	9.75 V	9,74 V	9,76 V				
IDN1	7,45MA	7.20MA	6.65MA	6.80MA				
IDNS	18.8MA	17.1MA	14 8MA	15.2MA				
IDP1	-2.99MA	-3,04MA	-2.96MA	-3,04MA				
IDP2	=5.76MA	-5.79MA	-5.58MA	-5.82MA				
IOZi	2.90NA	3,10NA	1.40NA	3.99NA				
IOZZ	6.20N4	-400.PA	4.90NA	500 PA				
1023	200.PA	4.90NA	-100_PA	3.80NA				
IOZ4	-100.PA	5.40NA	-1.50NA	5,70NA			•	
1025	6.10NA	-1.40NA	5.60NA	-1,10NA				
1076	6.00NA	-1,10NA	5.80NA	HI ZUNA				
1027	6.00NA	-1.30NA	5.60NA	-1,20NA				
1028	5.60NA	-1.20NA	5.60NA	-1.40NA				

11.6UA

-9.56MA -9.49MA -10.2MA

ILDP

IL1 IL2 IL3 IL4

i.h

RCA	CDP182280	256 X 4	CMOS STATIC	RAM 3	1 AUG 78	TEMP :	⇒55 C	SN:	56
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PASSED GALPAT			C210V		•		
PASSED GALPAT PASSED GALPAT	(TIGHT LIM (TIGHT LIM		CC=10V CC=5V			UCIBILITY O L. PAGE IS 1	
PASSED DATA RE	TENTION TES	Ţ				•	
		VCI	2 = 4.5	5 V	5.0	V	10°0v
ADDRESS ACCESS	TIME	(TAA)	249	n N	190	N	70.0N
DATA SETUP TIM		(TDS)		, ON	50.		B. GON
DATA HOLD TIME	.	(TDH)	8.4	9 Ø N	8.0	an	10.0N
ADDRESS SETUP	TIME	(TAS1)	12	ØN	8.0		4.00%
ADDRESS SETUP		(TAS2)		P.N	90.		38.QN
ADDRESS HOLD T		(HAH)	-1B,		-12,		2.00N
WRITE PULSE WI	וויךו	(TWP)	70.	. ØN	62,	MN	35.0N
CS1 SETUP TI		(TCSS1)		5.N	126	N	58,0N
		(TCSS2)		5 . N	118		56,0N
CS: HOLD TIM		(TCSH1)	38,	ØN	34.		55'0N
CSS HOLD TIM	16	(TCSH2)	42.	. ØN	36.	ΜN	20.05
OUTPUT ACTIVE	FROM CS1	(TDOA1)	248	2 N	190	Ī.N	82,0N
OUTPUT ACTIVE		(SAOUT)		7. N	188	N	85 WW
OUTPUT ACTIVE	FROM MRD	(TDOA3)	44,	.ØN	38.		55.0W
OUTPUT HOLD FR	ROM CS1	(TDOH1)	13	2.N	102	N	36,0N
- ՕՍԾԲԱԾ НՅԼԻ ԲԶ		(SHOGT)		2 N	102	LN .	36, QN
OUTPUT HOLD FA		(EHOQT)	134	4,N	112	N ۾	26,0N
OUTPUT HOLD FR	-	(TPDH)		E.N	108	- N	26.0N
READ CYCLE TIM		(TRC)		4 . N	192	P.N	104.N
WRITE CYCLE TI	(ME	(TWC)	201	B.N	176	· · · ·	96.0N
IIL	IIH		VICI		VICP		
A 0 0 0 0A			3.09		-3,09	V	
A1 =100.PA			3.12			V	
A2 0,00 A	•		3,13		-3,15		
A3 =100.PA	v 0.00	Α	3.14	٧	-3,14	V	
A4 Ø.00 A			3,12		-3,13		
A5 -100.PA			3.08		-3,10	V	
A6 -100.PA			3,08		-3,10	V	
A7 =100.PA	100.	PA	3.09	V	-3 ,13	V	
CS1 -100.PA			3,13		-3,12	y	
C\$2 -100.PA			3.13		-3,14	V	
MWR #100,PA MRD =200,PA			3,10		-3.14 -3.10 -3.11	V	
rasa =eun∍en	_		3.11	٧		٧	
0.00 0.00			3.16			V	
011 -100.PA			3.16		-3,11	V	
DIS -100.PA			3.16		-3,11	V	
DI3 0.00 A	100.	H A	3.14	٧	⇒3.1 0	V	
			B-25	5			

RCA	CDP1822SD	as6 x 4 cmos	STATIC RAM	31 AUG 78	TEMP:	₩55 C SN:
					PAGE	6 OF 10
	ngg	001	soa	D03		
VOLS	90.0MV	95.ØMV	100.MV	100, MV		
VOL2	95.0MV 4.88 V	110.MV 4.89 V	130.MV 4.88 V	135.HV 4.88 V	1 54	
And	9,79 V	9.79 V	9.78 V	9,79 V	* * H	
IDN1	AMMS.8	7.90MA	7.35MA	7.50MA		
IDN2	20,9MA	19.2MA	16.8MA	17.2MA		
1065	₩3.42MA ₩6.76MA	=3.49MA =6.86MA	=3.46MA =6.64MA	#3,52MA #6.90MA		
1 m / L	- 4.8 - 10.11.	- Wareh	·· O # () + / / /			
1071	4.8ØNA	-1.50NA	4.70NA	-3, 20NA		
1025	900.PA	1 - 70NA	1.30NA	400 PA 2 00NA		
1023	5.50NV	1,30NA	400.PA	ANDB'S		
1024	5.70NA	-1.80NA	4.20NA	-1,40NA		
1025	-1,40NA	4.20NA	-1.50NA	3,79NA		
1026	-1.50NA	4,90NA	-1.90NA	4,10NA		
1027	-1.76NA	5,10NA	WS BONA	4,90NA		
IOZB	-1,80NA	5.20NA	ANDE.S-	5.00NA		
		•				
ILOP	7 _. 60UA					
ILi	-10.2MA					
ĭĽZ	-10.2MA					
IL3	=10,2MA					
IL4	e10€2M∧					

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RCA	CDP1822SD	256 X 4	CMOS STATIC RAM	31 AUG 78	TEMP:	85 C	SN:	26

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PASSED	GALPAT	(WINE	LIMITS)	VCC=1ØV
PASSED	GALPAT	CTIGHT	LIMITS)	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS)	VCC=5V

	vec	= 4.5 V	5.0V	10.0v
AUDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA) (TDS) (TDH)	245.N 20.0N 14.0N	210.N 16.0N 14.0N	90'.0N 8.00N 14'.0N
ADDRESS SETUP TIME ADDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WINTH	(TAS1) (TAS2) (TAH) (TWP)	8.00N 118.N -18.0N 74.0N	8.00N 102.N -14.0N 66.0N	46.00 4.600 25.00 4.600
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS1) (TCSS2) (TCSH1) (TCSH2)	160.N 158.N 44.0N 48.0N	142, N 140, N 40, NN 42, NN	74,0N 72,0N 76,0N 26,0N
OUTPUT ACTIVE FROM CS OUTPUT ACTIVE FROM MR	(SADOT) S	240.N 238.N 56.0N	208,N 206.N 50.0N	104.N 102.N 30.0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH1) (TDOH2) (TDOH3) (TPOH) (TRC) (TWC)	146.N 142.N 138.N 134.N 264.N 216.N	116, N 114, N 116, N 112, N 232, N 200, N	44,0N 44,0N 28,0N 30.0N 112.N 128.N
IIL	11H	VICI	vica	
A1 -20,8NA A2 -18,4NA	19.8NA 18.8NA 19.7NA 18.4NA	2.71 V 2.75 V 2.76 V 2.78 V	#2,72 V #2,75 V #2,80 V #2,78 V	
A5 =18.5NA A6 =19,0NA	20,7NA 19,2NA 20,7NA 20,2NA	2,76 V 2.70 V 2.71 V 2.73 V	22,78 V 22,73 V 22,73 V 22,76 V	
CS2 =21,0NA MWR =21,0NA	23.2NA 22.3NA 20.1NA 21.2NA	2.75 V 2.77 V 2.73 V 2.73 V	52,76 V 52,81 V 52,74 V 52,76 V	
DI1 =19.5NA DI2 =21.7NA	21.7NA 21.9NA 22.3NA 23.7NA	2.80 V 2.80 V 2.80 V 2.79 V	#2,75 V #2,75 V #2,75 V #2,75 V	

RCA	CUP1892SD	256 X 4 CMBS	STATIC RAM	31 AUG 78	TEMP	85 C	SN:	26
					PAGE	8 OF	10	
	000	001	507	003				
A0175	130 MV 145 MV	135,MV 170,MV	150,MV 205,MV	145, MV 205, MV 4, 81 V				
2H0A	4,81 V 9,64 V	4.82 V 9.64 V	4.80 V 9.62 V	4,81 V 9,64 V				
IDN1	5.65MA 13.7MA	5.45MA 12.4MA	5.05MA 10.6MA	5,15MA 17,8MA				
IOP1	-2,11MA -3,78MA	⇒2,14MA =3.75MA	AME0.5-	=2,14MA =3.79MA				
IOZ1	65.5NA 59.9NA	44.5NA 38.7NA	43.7NA 43,1NA	37.5NA 33.5NA				
1023 1024	48,9NA 52.5NA	44.0NA 41.7NA	34,2NA 35.7NA	39.8NA 37.9NA				
1025 1026 1027 1028	53.0NA 54.4NA 54.0NA 54.6NA	37.3NA 37.3NA 36.3NA 37.3NA	39,2NA 40,5NA 39,1NA	32,2NA 32,8NA 32,0NA				
		жис _е те	40.5NA	31 _* 8NA				
ILDP	Su.muA							
IL1 IL2 IL3 IL4	⇔8,53MA ⇔8,50MA ⇔10,2MA ⇔10,2M4							
* 14 -	-101004							

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PASSED GALPAT (WIDE LIMITS) VCC=10V PASSED GALPAT (TIGHT LIMITS) VCC=10V PASSED GALPAT (TIGHT LIMITS) VCC=5V

	vcc	= 4.5V	5.0V	10:0V
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA) (TDS) (TDH)	260.N 18,0N 16.0N	220°, N 16.0N 14.0N	105.N 8.90N 14.0N
ADDRESS SETUP TIME ADDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WIDTH	(TAS1) (TAS2) (TAH) (TWP)	4.00N 124.N -18,0N 78.0N	4.00N 110.N -16.0N 70.0N	4.00N 60 1N -4.00N 42.0N
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS1) (TCSH1) (TCSH1) (TCSH2)	172.N 170.N 46.0N 50.0N	150, N 150. N 42. ON 46. ON	82,00 78,00 26,00 26,00
OUTPUT ACTIVE FROM CS OUTPUT ACTIVE FROM CS OUTPUT ACTIVE FROM MR	(SADOT) S	256.N 254.N 62.ØN	224', N 252. N 56. MN	114,N 112.N 34.0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM CS2 OUTPUT HOLD FROM MWR OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TOOH1) (TOOH2) (TOOH3) (TPOH) (TRC) (TWC)	146.N 144.N 136.N 136.N 280.N 280.N	118, N 116, N 116, N 112, N 248, N 200, N	46,0N 46,0N 30,0N 120,N 136.N
IIL	IIH	VICI	V1C5	
A1 #118,NA A2 #111.NA	194, NA 195, NA 196, NA 192. NA	2.63 V 2,67 V 2.69 V 2.70 V	-2,64 V -2,68 V -2,73 V -2,71 V	
AS = 110.NA A6 = 113.NA	109,NA 102,NA 107,NA 105.NA	2.68 V 2.63 V 2.63 V 2.65 V	-2,71 V -2,65 V -2,66 V -2,69 V	
CS2 =120.NA MWR =114.NA	114, NA 115. NA 105, NA 110. NA	2.68 V 2.70 V 2.65 V 2.66 V	=2,68 V =2,74 V =2,66 V =2,68 V	
D11 = 105.NA D12 = 111.NA	108,NA 105.NA 108,NA 110.NA	2.73 V 2.73 V 2.73 V 2.71 V	=2,68 V =2,67 V =2,68 V =2,68 V	

RÇA	CDP1822SD	256 X 4	4 CMO	STATIC	RAM	31	AUG 78	TEMP	125 C	SN:	26

PΑ	rE	10	OF	10
PΔ	te E	נשנ	U.C	T V)

	Poø	ព្រក្	500	003
VUL 1	145.MV	155 MV	170.MV	165, MV
AOT 5	165.MV	190.MV	530°HA	235 MV
VOHI	4.78 V	4,78 V	4.78 V	4,78 V
VUH5	9.57 V	9° 57 V	9.56 V	9 <u>.</u> 57 V
IDN1	5.10MA	4,90MA	4,50MA	4,65MA
IDNS	12,2MA	10.9MA	9.35MA	9.50MA
IDP1	-1.87MA	-1.89MA	-1.83MA	9.50MA -1.89MA
IDPS	-3.20MA	-3.15MA	-3.00MA	-3-19MA
IOZi	73.3NA	20.1NA	-5.50NA	₩20°0kγ
1025	51,4NA	11.8NA	+14 BNA	=24 4NA
1023	50 2NA	-100.PA	-13,5NA	=35 8NA
TUZ4	44.6NA	_900 PA	+18.0NA	-36,9NA
1075	47.3NA	6.70NA	-15,7NA	-26,2NA
1026	44.6NA	1.60NA	-16,4NA	-31,2NA
1027	42.7NA	1,80NA	-17.0NA	-28.3NA
1028	40.4NA	-1.20NA	-18.8NA	-31.5NA
ILDP	BO OULA			
IL1	₩8.79MA			
ILS	-8.79MA			
IL3	-10.2MA			
71.4	1 M A A M A			

RÇA	CDP18225D	256 X 4	CMOS STATIC RAM	31 AUG 78	TEMP:	25 C	SN:	27
	• • • • • • • • • • • • • • • • • • • •	· ·						

PAGE 1 OF 10

	PASSED PASSED PASSED	GALPAT GALPAT	THRIT)	LIMITS) LIMITS) LIMITS)	VCC= VCC=	1 0 V	repr Origi	ducibi Nal 94	LITY OF THE GE IS POOR
:	PASSED	DATA RET	ENTION	TEST					
ä					ACC =	4.5V	5.	ρV	10.0V
1		ACCESS		(TAA)		255.N		5 N	85. ØN
b		TOP TIME		(TOS) (TDH)		24,0N 10.0N		_0N _0N	A. 70N 10.0N
-		SETUP T		(TAS1		12.0N		• ù V	4. PON
		SETUP T		(TAS2		127.N		ดไท	50.0N
-		HOLD TI		(TAH)	•	-18,0N	-16		-4.70N
7.	WRITE F	ULSE WID	нт	(TWP)		70.0N	53	.ON	36. QN
_	-	TUP TIM		(TCSS		166.N	1.4	۸, ۲	70,0N
		TUP TIM		CTCSS		165 N		Ø N	68, NN
ţ.		DLD TIME		(TCSH		38,0N		.ON	55° WN
	CS2 HO	ILD TIME		(TCSH	12)	40.0N	36	• UV	45°0M
	OUTPUT	ACTIVE F	ROM CS1	(TDOA	1)	244.N	20	4 , N	92,00
ŀ		ACTIVE F				240 N		e N	90,00
	DUTPUT	ACTIVE F	ROM MRD			54.0N		.ØN	26.0N
	DUTPUT	HOLD FRO	M CS1	(TDOH	11)	154.N	12	5 N	34,0N
		HOLD FRO		(Teah		150 N	11	8 N	34, ØN
		HOLD FRO		CTOOK	-	142 N	12:	8 N 8 N	30,0N
		HOLD FRO		(TPDH		138.N	4.4	4 N	32.00
to.		CLE TIME		(TRC)		264.N	3 2	4 N	120.0
		YOUF TIM		(TWC)		272.N		0.N	112.N
		TIL	r	IH.	V	IC1	AICS		
	AØ	-1.60NA	2	2.10NA -	2	.96 V	-2,97	V	
1.	Ai	-1.70NA	1	.70NA		.99 V	-3,01	V	
	45	-1.50NA		. BPNA		.96 V	42,98		
: 1	ĒΑ	⇒1.40NA	7	.10NA		.95 V	-2,97	٧	
-1-	Λ4	-1.90NA	1	,50NA	5	.97 V	2,99		
	A5	-2.10NA		, 90NA	5	.93 V	-2,9 5	٧	
	A6	₽1.80NA		, BONA	5	.91 V	÷2,93	٧	
	Δ.7	-1.60NA	1	60NA	5	.91 V	÷2,93	٧	
	CS1	-1.60NA	ä	2.20NA	5	.94 V	-2,94	٧	
,	csa	-2.50NA		ANDO		.96 V	=2,97	ν	
•	MWR	-2.90NA	1	.50NA			42,93		
,	MRD	-2.10NA	ä	. OONA	5	.91 V .92 V	≈2°,95	V	
:	DIO	-2.30NA	2	ANDS.	5	.98 V	-2 ¹ ,95	ν	
	DII	W1,80NA		10NA		.97 V	-2,91	v	
11	012	AZ.10NA		.90NA		na v		v	
	013	-2.20NA		40NA		98 V	-2.93		
ŗ.					E	3-261			

RCA	CDP18225D	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP	25 C	SN:	27
					PAGE	2 OF	10	
	noa	DO1	500	003				
00H2 VOL3 VOL3	110.MV 110.MV 4.84 V 9.78 V	110,MV 120.MV 4,84 V 9,79 V	120.MV 135.MV 4.84 V 9.78 V	120 MV 130 MV 4 85 V 9 79 V				
ION1 ION2 IOP1 IUP2	6,75MA 17.0MA -2,51MA -5,72MA	6,55MA 15,9MA -2,55MA -5,78MA	6.10MA 14.0MA ≈2.48MA ≈5.56MA	6.25MA 14.5MA 52.51MA 5.76MA				
1021 1022 1023 1024	40,6NA 42,8NA 38,4NA 35.8NA	47.4NA 43.0NA 45.5NA 47.8NA	44,6NA 47,0NA 45,8NA 42,9NA	36.8NA 33.0NA 8NA 8NA 808.8E				
1025 1026 1027 1028	43.6NA 44.0NA 43.2NA 42.8NA	41.9NA 42.0NA 42.1NA 41.3NA	50-2NA 49-4NA 49-1NA 48-4NA	31.7NA 31.3NA 31.4NA 31.7NA				
ILDP	≖5 "ØØUA							
IL1 IL2 IL3 IL4	-25,0UA -20,0UA -10,0UA -5,00UA							

PASSED	GALPAT	(WIDE	LIMITS)	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS)	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS	VCC=5V

	VCC	= 4.5V	5'.0V	10'.0V
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA) (TDS) (TDH)	265.N 28'.UN 8.00N	210'N 22.0N 8.00N	80 . 0N 8 . pon 10 . 0N
ADDRESS SETUP TIME ADDRESS SETUP TIME AUDRESS HOLD TIME WRITE PULSE WINTH	(1881) (58AT) (HAT) (GWT)	16.0N 120.N -18.0N 80.0N	12,0N 96.0N #14.0N 68.0N	4.00N 42.0N -2.0N 34.0N
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS1) (TCSS2) (TCSH1) (TCSH2)	164.N 158.N 38.0N 42.0N	138 N 134 N 32.9N 34.6N	20.0N 52.0N 62.0N 82.0N
OUTPUT ACTIVE FROM CS1 OUTPUT ACTIVE FROM MRD	(IADOT) (SAOOT) (EAOOT)	744.N 742.N 50.0N	198, N 186. N 42. AN	84,0N 82,0N 24.0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH1) (TDOH2) (TDOH3) (TPOH) (TRC) (TWC)	146.N 144.N 140.N 136.N 248.N	114'N 112'N 116'N 112'N 208'N 192'N	34,0N 34,0N 30,0N 30,0N 96.0N
TIL II	ſН	VICI	VICP	
A1 =300.PA 30 A2 =300.PA 30	70.PA 70.PA 70.PA .OONA	3.07 V 3.09 V 3.08 V 3.07 V	=3,06 V =3,10 V =3,09 V =3,08 V	
A5 -400.PA 50 A6 -400.PA 40	70.PA 70.PA 70.PA	3.09 V 3.04 V 3.03 V 3.03 V	=3.10 V =3.06 V =3.05 V =3.04 V	
CS2 =600.PA 30 MWR =700.PA 20	20°.РА 20°.РА 70°.РА 70°.РА	3.06 V 3.09 V 3.02 V 3.04 V	-3,06 V -3,08 V -3,04 V -3,06 V	
DI1 -400.PA 40	00.PA 00.PA 00.PA 00.PA	3.11 V 3.10 V 3.12 V 3.11 V	-3.06 V -3.08 V -3.05 V -3.04 V	
		- a/a		

RCA	CDP18888D	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP:	⇔20 C	SN:	27
					PAGE	4 OF	10	
	000	001	500	003				
VOL1 VOL2 VOH1	100,MV 95,0MV 4,88 V 9,82 V	100.MV 105.MV 4.88 V 9.82 V	105.MV 115.MV 4.87 V 9.81 V	105,MV 115,MV 4,87 V 9,82 V				
IDN1 IDN2 IDP1 IDP2	-2.99MA	7.35MA 18.3MA -3.00MA -6.79MA	6.85MA 16.1MA -2.94MA -6.61MA	7.00MA 16.8MA -3.00MA -6.84MA				
1071 1022 1023 1024	2,60NA	6,20NA A 10,20 A 15,01 A 15,0NA	7.40NA 10.7NA 4.30NA 3.60NA	4, 90NA 1, 90NA 6, 70NA 7, 90NA			·	
1025 1026 1027 1028	8.70NA 8.80NA 9.00NA ANQP.8	3,00NA 3,30NA 3,00NA 3,10NA	10,6NA 10,8NA 10,7NA 10.8NA	1,20NA 1,20NA 1,30NA 1,30NA				
1LDP	800.NA							
IL1 IL2 IL3 IL4	-70,0UA -15,0UA -5,00UA	·						

RCA	CDP1822SD	256 X 4	CMOS	STATIC RAN	31	AUG	78	TEMP:	#55 C	: SN:	27
								PAGE	5 OF	10	

PASSED	GALPAT	(WIDE	LIMITS)	ACC=10A
PASSED	GALPAT	(TIGHT	LIMITS)	VCC=10V
PASSFD	GALPAT	THOIT)	LIMITS	VCC=5V

PASSED DATA RETENTION	TEST			
	vec	= 4.5V	5.0v	10.0V
AUDRESS ACCESS TIME	(TAA)	260.N	205, 6	70'.ØN
DATA SETUP TIME	(TDS)	34.0N	26.0N	a røn
DATA HOLD TIME	(TDH)	8.00N	8.00N	10.0N
DATA HOLD TIVE	Clung	C . VIBIA	O ♥ Ø WiA	1 6 - 610
AUDRESS SETUP TIME	(TAS1)	14.0N	10,0N	4.00N
ADDRESS SETUP TIME	(TAS2)	116.N	92.0N	40.0N
ADDRESS HOLD TIME	(HAT)	-18, ON	-14.0N	-2,00N
WRITE PULSE WINTH	(TWP)	88 QN	60.0N	32.0N
and a complete market		a mar a la la	4 15 11 1 4	(at au
CS1 SETUP TIME	(TCSS1)	156 N	134 N	60,0N
CSS SETUP TIME	(TOSS2)	164.N	130.N	58,0N
CS1 HOLD TIME	(TCSH1)	38, UN	40.PN	20,0N
GS2 HOLD TIME	(TCGH2)	52.0N	42.9N	18.0N
DUTPUT ACTIVE FROM CS1	(TDGA1)	248 N	194 N	80,0N
DUTPUT ACTIVE FROM CS2		246 N	192.N	8ต.์ตก
OUTPUT ACTIVE FROM MRD		46.0N	40.0N	40°08 40°08
			1.	+
OUTPUT HOLD FROM CS1	(TDOH1)	142.N	108 N	32,0N
OUTPUT HOLD FROM CS2	(LDUH5)	138,N	106 N	32,0N
OUTPUT HOLD FROM MRD	(TOOH3)	138.N	106 N 116 N	28,0N
OUTPUT HOLD FROM MWR	(TPDH)	136 N	118, N 200, N	30.0N
READ CYCLE TIME	(TRC)	232.N	200, N	164.N
WRITE CYCLE TIME	(TWC)	224.N	Suu'n	96.0N
iir i	Ін	vini	A1C5	
S V 00°N 08	AG PA	3.16 V	-3,15 V	
	ดด⊊PA	3.17 V	-3,19 V	
= '	00 PA	3.17 V	-3-19 V	
	ON PA	3.17 V	#3,19 V #3,18 V	
	du di Tari	por ¹ a sec		
	OU.PA	3.19 V	-3,20 V	
	00,P4	3.13 V	-3,16 V	
	00,PA	3.13 V	-3,15 V	
A7 =100.PA 1	OO.PA	3_13 V	-3.15 V	
CS1 -100.PA 1	пп _РА	3.17 V	-3,16 V	
CS2 -200,PA 1	MU PA	3.19 V	-3,18 V	
	DO PA	3.13 V	+3,15 V	
	00.PA	3.15 V	∞3.17 V	
858 486 5	en en 'en a	Maria de la	- 1	
DIO =100.PA 1	ØØ, PA	3.21 V	#3,16 V	
	OO, PA	3.20 V	#3,13 V	
	MM.PA	3.22 V	#3,15 V	
DI3 =100.PA 1	ng.pa	3.21 V	⇔3,14 V	

RCA	CDP1822SD	256 X 4	CMOS STA	TIC RAM	31	AUG 78	TEMP:	e55 C	SN:	27
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PAGE	6	OF	10
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	noø	DOI	2005	503
VOL 1	90° 6MV	90.0KV	100 MV	95.0MV
VOL 3	85.0MV	95.PMV	105.MV	100 MV
VUH1	4 88 V	4,89 V	4.88 V	4,89 V
AOHS	9 84 V	9.84 V	9.84 V	9.84 V
IDNI	8.15MA	7,95MA	7,45MA	7',55MA
10N5	21.4MA	SO SWA	18 0MA	18.6MA
IDP1	-3.37MA	-3.45MA	™3.40MA	-3.44MA
IDP2	-7,7@NA	-7.88MA	#7.59MA	-7.84MA
1021	#200,PA	5 80NA	-1,10NA	5,30NA
1025	2.70NA	2,50NA	1,30NA	2.70NA
1073	2.50NA	1,40NA	3.20NA	100 PA
1024	-700.PA	5.10NA	#100 PA	3.70NA
1025	4.80NA	~100.PA	4,20NA	200,24
1026	5.10NA	200 PA	3.70NA	400 PA
IOZ7	4 60NV	300 PA	3 80NA	600 РА
1078	4.70NA	400 PA	3.40NA	600 PA
ILDP	⊶3,40UA			
IL1	-20,0UA			
ILS	≈15.0UA			
1L3	95.00UA			
IL4	₩5.00UA			

PAGF 7 OF 10

PASSED GALPAT (TIGHT	LIMITS) VC LIMITS) VC	C=10V C=10V C=5V	REPRODUCIB ORIGINAL PA	ility of the Lee is fook
	vcc	≈ 4,5∨	5 . 0V	10.0v
ADDRESS ACCESS TIME	(TAA)	255.N	215,N	90',0N
DATA SETHP TIME	(TDS)	26,0N	20,0N	N00,8
DATA HOLD TIME	(HDT)	12.0N	12,0N	12.0N
AUDRESS SETUP TIME	(TAS1)	8.00N	8'.09N	4.00N
ADDRESS SETUP TIME	(TAS2)	122.N	196.N	54.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-16.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	80.0N	70.0N	40.0N
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS1)	174.N	148, N	74,0N
	(TCSS2)	172.N	148. N	74,0N
	(TCSH1)	48.0N	44. M	26,0N
	(TCSH2)	54.0N	46. MN	26.0N
OUTPUT ACTIVE FROM CS OUTPUT ACTIVE FROM MR	(SADOT) SE	244.N 742.N 56.ØN	212.N 210.N 50.0N	102.N 102.N 28.0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRO OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH1) (TDOH2) (TDOH3) (TPOH) (TRC) (TWC)	156.N 152.N 142.N 140.N 272.N 232.N	124, N 122, N 120, N 116, N 232, N 208, N	40,0N 40,0N 34,0N 36,0N 120,N
111	IIH	vici	VICA	
AD =18.1NA A1 =18.2NA A2 =15.1NA A3 =14.8NA	20.3NA 18.9NA 15.8NA 27.1NA	2.93 V 2.92 V 2.93 V	-2,94 V -2,99 V -2,94 V -2,93 V	
A4 =16.8NA	15.4NA	2.93 V	=2,95 V	
A5 =18.6NA	17.3NA	2.89 V	=2,91 V	
A6 =17.5NA	17.5NA	2.88 V	=2,89 V	
A7 =15.9NA	16.3NA	2.87 V	=2,89 V	
CS1 -17,0NA	17.4NA	2.90 V	2,90 V	
CS2 -16,9NA	17.3NA	2.93 V	2,93 V	
MWR -17,3NA	15.1NA	2.87 V	2,89 V	
MRD -17,0NA	16.0NA	2.88 V	2,91 V	
DIØ =16,3NA	16.8NA	2.93 V	=2'91 V	
DII =15,3NA	15.8NA	2.93 V	=2'86 V	
DIZ =15,6NA	15.7NA	2.95 V	=2'90 V	
DI3 =15,6NA	16.7NA	2.94 V	=2'89 V	

RCA	CDP18225D	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP:	85 C	SN
					PAGE	8 OF	10
	nga	001	Son	p03	ì		
VOL 1	125.MV	130,MV	140.MV	135, MV			
Aurs	130.MV	140.MV	160 MV	150 MV			
VOH1	4.82 V	4 82 V	4.82 V	150 MV 4 82 V			
AOHS	9.74 V	9.75 V	9.74 V	9.75 V			
IDNi	5,95MA	5.75MA	5°,35MA	5,45MA			
IONS	14.8MA	13.7MA	12.1MA	12.5MA			
IDP1	+2.15MA	-2.18MA	-2,12MA	-2,15MA			
IDP2	-4.88MA	=4.93MA	-4.74MA	-4-94MA			
1021	371.NA	386 NA	375 NA	ANZPOE			
IOZZ	363.NA	391,NA	375.NA	303,00			
IDZ3	363.NA	387.NA	372,NA	396.NA			
10Z4	356.NA	390.NA	376.NA	299.NA			•
1075	364.NA	395 NA	379.NA	311, NA			
1026	364.NA	388, NA	392.NA	299, NA			
10Z7	373.NA	386 NA	381,NA	308, NA			
IOZ8	362.NA	393 NA	378.NA	299,NA 308,NA 302,NA			
TIND	// Cralla						
ILDP	4.8ØUA						
ILi	-35,0UA						
IFS	₩35.0UA						
11.3	-30.0UA						
114	⇔20,0UA						
-	-						

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RCA	CDP1822SD	256 X 4	CMOS STATIC RAM	31 AUG 78	TEMPS	125 C	SNI	27

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PASSED	GALPAT	(WIDE	LIMITS)	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS)	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS)	VCC#5V

	vcc	≈ 4.5V	5.0V	10.0v
ADDRESS ACCESS TIME	(AAT)	255.N	220'N	160.N
DATA SETUP TIME	(TDS)	26.0N	55.0N	8.00N
DATA HOLD TIME	(TDH)	14.0N	14.0N	14.0N
ADDRESS SETUP TIME	(TAS1)	4.00N	4. 99N	4 . 00H
ADDRESS SETUP TIME	(SRAT)	158 N	114.N	60,0N
ADDRESS HOLD TIME	(TAH)	-18,0N	=16. AN	-4.00N
WRITE PULSE WINTH	(TWP)	86.ØN	76 # ØN	44, ØN
CS1 SETUP TIME	(TCSS1)	180.N	156°N	82,01
CS2 SETUP TIME	(TOSS2)	178.N	154.N	78,0h
CS: HOLD TIME	(TCSH1)	54,0N	46.0N	۸0م'85
CS2 HOLD TIME	(TCSH2)	56.0N	50.0N	88.0N
OUTPUT ACTIVE FROM CS:	(TODA1)	256.N	224.N	112°N
OUTPUT ACTIVE FARM CS2	(SABOT)	254.N	888.8	110 N
OUTPUT ACTIVE FROM MRD	(EADOT)	60.0N	54.0N	30.0N
DUTPUT HOLD FROM CS1	(TOOH!)	158.N	128, N 124, N 122, N	44, ØN
OUTPHT HOLD FROM CS2	(SHOOT)	154 N	124,N	44, ØN
DUTPUT HOLD FROM MRD	(TDOH3)	142 . N	128,N	36,0N
OUTPUT HOLD FROM MWR	(TPDH)	142.N	N م 116	38 BN
READ CYCLE TIME	(TRC)	280.N	240 N	120 N
WRITE CYCLE TIME	(TWC)	240.N	216.N	136 N
IIL IIH	İ	VIC1	AICS	
AU -103,NA 107	.NA	2'91 V	-2,93 V	
	NA	2.95 V	-2.98 V	
· • ·	8NA	2.89 V	-2,9A V -2,91 V	
	.NA	2.88 V	== 90 V	
A4 #88.5NA 84.	3NA	2.89 V	- €2,93 V	
	9NA	2.87 V	€2,89 V	
	ØNA	2.84 V	#2,86 V	
	2NA	2.83 V	=2 85 V	
CS1 -92,3NA 85.	6NA	2.86 V	-2,87 V	
CS2 -90.1NA 88.	9 N A	2,89 V	<u>-</u> 2,90 V	
	BNA	8,83 V	⊕2,85 V	
MRD #90,0NA 85.	2NA	2.84 V	-2,8A V	
	2NA	2 A9 V	e 2 ,87 v	
	7NA	2,89 V	#2,82 V	
DI2 -84,0NA 82.	3NA	5.95 V	+2,86 V	
DI3 -80.4NA 80.	9NA	2.90 V	≈2.85 V	
		D 0/0		

RÇA E	000182250	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMPS	125 C SN:
					PAGE	10 OF 10
	noa	DO1	500	003		
VOL 1 VOL 2 VOL 1	140.MV . 3.MV 4.3. 1 9.72 V	145 MV 155 MV 4,80 V 9,72 V	155.MV 180.MV 4.80 V 9.70 V	150.MV 170.MV 4.80 V 9.72 V		
IDN1 IDN2 IDP1 IDP2	5.35MA 13.2MA *1.96MA -4.42MA	5.20MA 12.2MA -1.96MA -4.43MA	4.85MA 10.8MA +1.91MA -4.24MA	4.95MA 11.2MA =1.96MA =4.47MA		
1021 1022 1023 1024	1.51UA 1.51UA 1.50UA 1.49UA	1,58UA 1,57UA 1,57UA 1,57UA	1,53UA 1,53UA 1,53UA 1,53UA	1,25UA 1,25UA 1,26UA 1,25UA		
1025 1026 1027 1028	f.51UA 1.52UA 1.50UA 1.51UA	1,59UA 1,60UA 1,59UA 1,58UA	1.56UA 1.55UA 1.54UA 1.55UA	1,28UA 1,27UA 1,28UA 1,27UA		
ILDP	5.00UA					
IL1 IL2 IL3 IL4	#85,011A #95,011A #85,011A #85,011A					

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			PAG	F 1 OF 10
PASSED GALPAT (TIGHT	r LIMITS) Vo	CC=10V CC=10V CC=5V	REPRODUCIBILIT ORIGINAL PAGE	Y OF THE
PASSED DATA RETENTION	TEST			
	vac	= 4.5V	5. ev	10'.0v
AUDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA) (TDS) (TDH)	245 N 26 M 10 ON	205'N 22.0N 10.0N	80.0N 8.70N 10.0N
ADDRESS SETUP TIME ADDRESS SETUP TIME AUDRESS HOLD TIME	(TAS1) (TAS2) (TAH)	16.0N 120.N =18.0N	12.0N 98.0N -14.0N	4.70n 48.0n -2.70n
WRITE PULSE WINTH	(TWP)	68₌ØN	60.0N	36.0N
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS1) (TCSS2) (TCSH1) (TCSH2)	164.N 169.N 42.0N 46.0N	136,N 134.N 38.GN 38.GN	64', 0N 62', 0N 24', 0N 22', 0N
OUTPUT ACTIVE FROM CS OUTPUT ACTIVE FROM CS OUTPUT ACTIVE FROM MR	(SAOOT) SE	230.N 226.N 50.0N	194, N 192. N 44. MN	88,0N 88,0N 26.0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH1) (TDOH2) (TDOH3) (TPDH) (TRC) (TWC)	146 N 144 N 140 N 134 N 264 N	116,N 112,N 118, N 112,N 216,N	30,000 30,000 30,000 30,000 312,000
111	IIH	VICI	VICP	
A0 =3.40NA A1 =3.50NA A2 =3.40NA A3 =3.20NA	3,40NA 2,90NA 3,10NA 3,40NA	3.23 V 3.31 V 3.31 V 3.29 V	-3,23 V -3,29 V -3,37 V -3,34 V	
A4 =3.30NA A5 =2.80NA A6 =3.80NA A7 =3.40NA	3.20NA 2.90NA 3.60NA 3.20NA	3.36 V 3.23 V 3.22 V 3.21 V	-3,39 V -3,25 V -3,24 V -3.23 V	
CS2 -3.70NA MWR -3.20NA	3,50NA 3,50NA 3,10NA 3,40NA	3.27 V 3.31 V 3.28 V 3.26 V	-3,28 V -3,35 V -3,30 V -3,26 V	
DI1 -3.40NA	3,00NA 3,10NA 3,40NA 3,20NA	3.31 V 3.30 V 3.34 V 3.35 V	-3,29 V -3,25 V -3,26 V -3,28 V	

RCA	CDP1822SD	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP:	25 C	SNa	28
					PAGE	3 OF	10	
	nge	DO1	200	003				
VOL 1	90.0MV	95.0MV	105,MV	100, MV				
VÜL 2	100.MV	105.MV	120 MY	120.MV				
VOHI	4.85 V	4 85 V	4 84 V	4,85 V				
VOHS	9.79 V	9.80 v	9.78 V	4,85 V 9,80 V				
IDN1	7.95MA	7'.70MA	7.20MA	7.20MA				
IDNS	19.3MA	17.8MA	15.7MA	16.0MA				
IDP1	-2.58MA	-2.62MA	42.50MA	-2,56MA				
IDP2	=5.88MA	-5.99MA	-5.64MA	-5.96MA				
1071	46.1NA	56.8NA	53,1NA	46.7NA				
1025	42.7NA	60.2NA	49,5NA	50,0NA				
1023	48.7NA	54.2NA	54,6NA	45.3NA				
1024	48 1 NA	53,5NA	55.3NA	43,9NA				
1075	42.2NA	60.9NA	48 6NA	52,1NA				
1076	42.2NA	60.9NA	48,8NA	51.8NA				
1027	42.4NA	61.0NA	48.3NA	51.6NA				
1028	41.9NA	60.7NA	48.7NA	51.5NA				

ILDP

IL1 IL2 IL3 IL4 -5.00UA

-5.00HA -5.00HA -20.0UA ei e

(T)

PAGE 3 OF 10

PASSED	GALPAT	(WIDE	LIMITS)	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS	VCC#1ØV
PASSEU	GALPAT	(TIGHT	LIMITS)	VCC=5V

PASSED DATA RETENTION TEST

	VCC	# 4.5V	5.0V	10.0v
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA) (TDS) (TDH)	270.N 30.UN 8.00N	215'.N 24.0N 8.00N	75.0N 8.00N 8.00N
ADDRESS SETUP TIME ADDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WIDTH	(TAS1) (TAS2) (TAH) (TWP)	22.0N 126.N -18.0N 72.0N	16.0N 100.N =14.0N 64.0N	4.00N 42.0N -2.00N 32.0N
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS1) (TCSS2) (TCSH1) (TCSH2)	160.N 158.N 36.0N 38.0N	134, N 132, N 30, GN 32, GN	50.0N 55'0N 60'0N 65'0N
OUTPUT ACTIVE FROM CS OUTPUT ACTIVE FROM CS OUTPUT ACTIVE FROM MR	(SADOT) S	242N 238N 48ØN	196, N 194. N 42. DN	82,0N 80,0N 24.0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH1) (TDOH2) (TDOH3) (TPOH) (TRC) (TWC)	142.N 138.N 138.N 134.N 256.N 264.N	110, N 108, N 116, N 110, N 208, N 184, N	0.0E 0.0E 0.0E 00.0E 00.0E
	IIH	VIC1	V1CS	
A1 +400.PA A2 +400.PA	300 PA 300 PA 300 PA 400 PA	3.26 V 3.34 V 3.34 V 3.32 V	+3,32 V +3,31 V +3,38 V +3,36 V	
A5 -300.PA A6 -500.PA	300 PA 300 PA 600 PA 300 PA	3.38 V 3.25 V 3.25 V 3.23 V	+3,40 V +3,27 V +3,27 V -3,25 V	
CS2 -500.PA MWR -400.PA	400,PA 400,PA 300,PA 300,PA	3.30 V 3,34 V 3,30 V 3,29 V	=3,30 V =3,37 V =3,33 V =3,28 V	
DI1 -500.PA DI2 -300.PA	300.PA 300.PA 400.PA 300.PA	3.34 V 3.32 V 3,36 V 3.37 V	-3,31 V -3,27 V -3,28 V -3,30 V	

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RCA	CDP18225D	256 X 4	CMOS	STATIC RAI	1 31	AUG 7	8 TEMP	⇒20 C	SN:	28
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PAGE	U	OF	10

	noø	001	בסת	D03
VOL.1 VOL.2	85.0MV 85.0MV 4.87 V	85.0MV 95.0MV 4.88 V	90.0MV 105.MV 4.87 V	9m.gmv 1g5.mv 4,88 v
NOHS	9.85 A	9.83 V	9.82 V	9'.83 V
IDN1 IDN2 IDP1 IDP2	8.80MA 21.9MA -3.01MA -6.91MA	8.55MA 20.4MA -3.10MA -7.09MA	8.05MA 18.0MA -2.98MA -6.72MA	8.00M5 AME.81 AME03E= AME0.7=
1071 1022 1023 1024	10.7NA 7.80HA 4.10NA 7.50NA	6.00NA 6.60NA 11.1NA 7.60NA	10.8NA 9.00NA 4.20NA 7.40NA	3',40NA 3',50NA 9',30NA 6',00NA
1025 1026 1027 1028	5,10NA 5,10NA 4,90NA 4,80NA	9,60NA 9,20NA 9,90NA 9,60NA	6.70MA 6.50MA 6.30MA 6.10MA	5,70NA 6,20NA 5,90NA 6.30NA
ILDP	-1.80UA			
IL1 IL2 IL3 IL4	-5.00UA -5.00UA -20.0UA -15.0UA			

PAGE 5 OF 10

PASSED	GALPAT	(MIDE	LIMITS)	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS)	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS	VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

	vcc	= 4 _* 5V	5.0v	10'.0v
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA) (TOS) (TOH)	275.N 40.0N 6.00N	210.N 28.0N 6.00N	70.0N 8.00N 8.00N
ADDRESS SETUP TIME AUDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WINTH	(TAS1) (TAS2) (TAH) (TWP)	24.0N 126.N -18.0N 82.0N	16.7N 170.N =14.7N 66.7N	4.90N 40.0N ~2.00N 32.0N
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS1) (TCSS2) (TCSH1) (TCSH2)	164.N 162.N 42.0N 40.0N	134,N 132,N 36.AN 38.AN	56.6N 56.6N 56.6N 56.6N
OUTPUT ACTIVE FROM CS1 OUTPUT ACTIVE FROM CS2 OUTPUT ACTIVE FROM MRD	(1AGGT) (SAGGT) (EAGGT)	244 N 244 N 46 ON	192, N 190. N 38. ON	55.0N 80.0N 85.0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH1) (TDOH2) (TDOH3) (TPOH) (TRC) (TWC)	138, N 136, N 138, N 134, N 240, N 256, N	104', N 102', N 116', N 110', N 200', N 208', N	30,0N 30,0N 28,0N 28.0N 104.N 96.0N
IIL II	Н	VIC1	vice	
A1 -100.PA 10 A2 -100.PA 10	0,PA 0,PA 0,PA 0.PA	3.31 V 3.38 V 3.38 V 3.37 V	93,30 V 93,36 V 93,42 V 93,49 V	
A5 -100.PA 10 A6 -100.PA 20	0,PA 0,PA 0,PA 0,PA	3.42 V 3.30 V 3.30 V 3.29 V	-3,44 V -3,32 V -3,31 V -3,39 V	
CS2 =100.PA 10 MWR =100.PA 10	0.PA 0.PA 0.PA 0.PA	3,36 V 3,39 V 3,36 V 3,35 V	53,36 V 53,40 V 53,38 V 53,33 V	
DI1 -100,PA 10 DI2 -100,PA 10	0.PA 0.PA 0.PA 0.PA	3.38 V 3.38 V 3.41 V 3.41 V	=3,36 V =3,31 V =3,33 V =3,35 V	

RÇA	CDP182280	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP:	∍55 C	SN:	28
					PAGE	6 QF	10	
	សុល្ល	001	bos	003				
VOLI	80.0MV	VMN.98	85 ØMV	85.0HV				
VOLE	RO OMV	85.0MV	95 gMV	95,0MV				
ADH	4.88 V	4,89 V	4,89 V	4 89 V 9 85 V				
SHOV	9.85 V	9 85 V	9'_84 V	ע כמייב				
ION1	9,45MA	9 20MA	8.70MA	8,65MA				
IDN2		22.4MA	19.9MA	20.4MA				
IPP1	-3.46MA	#3 ₂ 57MΛ	-3.44MA	-3,46MA				
IDP2		-8.17MΔ	-7.75MA	#8 # 09M∆				
IQZ1	6.60NA	-300,PA	5.6ØNA	-900,PA				
1072		500.PA	a. aana	-900.PA				
1023		4.50NA	-600.PA	4 <u>,</u> 40NA				
IUZ4	4.00NA	900 . PA	3.10NA	1.DONA				
1025	500.PA	3.80NA	1.20NA	1,80NA				
1076		3.60NA	900.PA	2,20NA				
1027	300.PA	4,10NA	1.00NA	E, GONA				
1028	300.PA	3.70NA	800.PA	2.40NA				
ILOP	10.004							
TL 1	≈5.00HA							
ILS	-5.00UA							
IL3	-15.0UA							
114	m15 0UA							

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PASSED	GALPAT	(WIDE	LIMITS)	VCC=1@V
PASSED	GALPAT	(TIGHT	LIMITS)	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS	VCC≥5V

PASSEU DATA RETEN	ITOM IEDI			
	VCC	: = 4.5V	5.Øv	10'.0V
ADDRESS ACCESS TT	ME (TAA)	250.N	195.N	85, ØN
	(TDS)		55.UN	
DATA SETUP TIME		28,0N		8.00N
DATA HOLD TIME	(TpH)	15,0N	12.AN	1 = + 514
ADDRESS SETUP TIM	E (TAS1)	10.0N	<u>ล</u> ู้ดดูท	4.ØØN
			104 N	52,0N
ADDRESS SETUP TIME		120.N -18.0N	#1 4 " ህን! ቸው መጀመ	-5.60N
ADDRESS HOLD TIME		76 QN	68.0N	38.00
WRITE PULSE WINTH	() We J	10 2 61.4	És és 🛡 as ta	20 \$ 2014
CS; SETUP TIME	(TCSS1)	164.N	140 N	70, 0N
CS2 SETHP TIME	(TGSS2)	160 N	136 N	68,0N
CS1 HOLD TIME	(TCSH1)	46, ØN	42, ØN	26, ØN
CS2 HOLD TIME	(TCSH2)	50.0N	44.0N	26.0N
COME TOTAL PROPERTY	¢ (m tr) (to 2	30504		
OUTPUT ACTIVE FRO	M CSI (TDOA1)	224.N	196 N	98, ØN
DUTPUT ACTIVE FRO		N.454	194 N	96, ØN
DUTPUT ACTIVE PRO	-	50.0N	46.00	28.0N
and the best water a tea-	A CAMPAGE A			
OUTPUT HOLD FROM	csi (TDOH1)	146.N	116 N	34,0N 34,0N 30,0N
OUTPUT HOLD FROM		144.N	112,N	34.0N
OUTPUT HOLD FROM		138.N	118, N	30 . ON
OUTPUT HOLD FROM		134.N	112,N	32.0N
READ CYCLE TIME	(TRC)	256.N	224,N	120.N
WRITE CYCLE TIME	(TWC)	216.N	192 N	120 N
7777272	(11,00)			
IIL	IIH	VICI	AICS	
AØ =41,2NA	40.3NA ·	3.23 V	=3,24 V =3,30 V =3,38 V =3,35 V	
A1 =40.9NA	40.3NA	3.32 V	=3.30 V	
A2 -40,7NA	41. PNA	3.33 V	₩3.38 V	
A3 -41.8NA	42.0NA	3.31 V	≈3.35 V	
	W W			
A4 =41,4NA	41,9NA	3.38 V	-3,40 V	
A5 -38,8NA	39.8NA	3,24 V	-3,25 V -3,25 V	
A6 -41.8NA	41.1NA	3.24 V	-3,25 V	
A7 =41.5NA	40.6NA	3.55 A	-3,24 V	
804	um di i	7 40 11	7' 56 11	
CS1 -41.9NA	42.6NA	3.28 V	=3,29 V	
CS2 -43,0NA	44.3NA	3°35 A	-3,37 V	
MWR -41.0NA	42.1NA	3.29 V	-3,32 V	
MRD +42.0NA	43.1NA	3.27 V	-3.27 V	
DI0 -44.7NA	40.7NA	3.33 V	≈3° 30 V	
DI1 -4M.2NA	40.5NA	3.31 V	-3,26 V	
DI2 =39.6NA		3.35 V	±3,27 V	
	41 29NA		#3,30 V	
DI3 -39.5NA	40.5NA	3.36 V	#3.2V V	

RCA	CDP1822SD	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP:	85 C	SN:	28
					PAGE	8 OF	10	
	שטח	DO1	200	D03				
VQL 1	105.MV	105, MV	120,MV	115, MV				
AOLS	115.My	125.MV	145.MV	140.MV				
VOHI	4.82 V	4,82 V	4.82 V	140.MV 4,82 V				
ADHS	9.76 y	9,76 V	9.74 V	9.76 V				
IONI	7.05MA	6.80MA	6.35MA	6.35MA				
IDNS	16,7MA	15.4MA	13.5MA	.13.8MA				
IDP 1	#2,18MA	₩2.25MA	-2.14MA	-2,18MA				
IDP2	₩4.97MA	~5.12MA	-4.81MA	-5.03MA				
IOZI	372.NA	430, NA	419.NA	389, NA				
IOZZ	365.NA	421,NA	424 NA	381,NA				
1023	364.NA	425,NA	419.NA	386, NA				
1024	366.NA	418.NA	427.NA	AM. 585			4	
1025	367.NA	426 NA	431.NA	391, NA				
1026	380,NA	419,NA	430.NA	391, NA				
1027	370.NA	428,NA	420.NA	394,NA				
1078	368.NA	422.NA	431.NA	384 NA				
7. 15.55								
ILDP	⇔5.00UA							
IL 1	≈35 ,0UΛ							
IĽŠ	-40.PUA							
11.3	-50,0UA							
IL4	=45_0UA							
7.50 -1	~ ~ g ~ Q //							

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PASSED	GALPAT	(WINE	LIMITS)	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS)	VCC=10V
PASSEU	GALPAT	(TIGHT	LIMITS)	VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST								
	VCC	= 4.5V	5,0V	10.0V				
ADDRESS ACCESS TIME	(AAT)	N.BES	205 N	95. ØN				
DATA SETUP TIME	(TDS)	78,0N	25.UN	8.000				
DATA HOLD TIME	(YOH)	12.0N	12.0N	12.00				
AUDRESS SETUP TIME	(TAS1)	8.00N	A. OØN	4.901				
ADDRESS SETUP TIME	CYASED	124.N	112.N	58,ØN				
ADDRESS HOLD TIME	(TAH)	≈18,0N	-14.0N	4.00N				
WRITE PULSE WIDTH	(TWP)	78.ØN	70.0N	42.01				
CS1 SETUP TIME	(TOSS1)	162.N	142'N	76', ØN				
CSP SETUP TIME	(YCSS2)	158.N	140 N	74 AN				
CS1 MOLD TIME	(TCSH1)	48,0N	44.0N	28,0N				
CS2 HOLD TIME	(TCSH2)	52.0N	46.9N	28. ØN				
OUTPUT ACTIVE FROM CS	i (TDOA1)	234.N	208 N	110.N				
OUTPUT ACTIVE FROM CS		232.N	504 V	106.N				
OUTPUT ACTIVE FROM MR		54.0N	48.7N	30.0N				
B. (50) 5	4555			•				
OUTPUT HOLD FROM CS1	(TDOH1)	146.N	116, N	36,0N				
OUTPUT HOLD FROM CS2	(TOOHE)	144.N	114,N	36, ØN				
OUTPUT HOLD FROM MRD	(TDNH3)	138.N	118 N	34 ØN				
DUTPUT HOLD FROM MWR	(TPDH)	136.N	112 N	36.0N				
READ CYCLE TIME	(TRC)	256.N	224'N	120,N				
WRITE CYCLE TIME	(TWC)	P16.N	192.N	M.851				
IIL	IIH	VICI	VICE					
AØ -234.NA	229.NA	3,27 V	-3,28 V -3,35 V -3,48 V -3,39 V					
A1 #233,NA	231,NA	3.36 V	+3,35 V					
A2 -232.NA	231, NA	3.37 V	-3,42 V					
A3 -237.NA	235.NA	3.35 V	=3,39 V					
A4 =236.NA	237.NA	3.42 V	=3,45 V					
A5 #228.NA	227.NA	3.27 V	-3,29 V					
A6 #233.NA	231,NA	3,27 V	+3.28 V					
A7 =234.NA	227.NA	3.25 V	+3,28 V -3,27 V					
CS1 =243.NA	239 NA	3.32 V	-3,34 V					
CS2 -241.NA	246.NA	3.36 V	-3,41 V					
MWR -236.NA	239 NA	3,33 V	=3,36 V					
MRD =241.NA	240.NA	3.31 V	=3.31 V					
DIØ #234.NA	231,NA	3,37 V	-3,35 V					
DI1 -227.NA	231,NA	3.35 V	-3,3% V					
DI2 -229.NA	233,NA	3,39 V	-3,31 V					
DI3 =28.NA	232.NA	3.40 V	=3.34 V					
= -: · · · · · · · · · · · · · · · · · ·		B-279	· ·					

RCA	CDP18225D	256	X 4	CMOS	STATIC	RAM	31	AUG	78	TEMP:	125	C	SN:	85
										PAGE	10 0	F	10	

	nga	DOI	500	003
VOL1 VOH1 VOH2	115.MV 125.MV 4.80 V 9.72 V	120,MV 140,MV 4,80 V 9,72 V	130.MV 160.MV 4.80 V 9.71 V	130 MV 155 MV 4,80 V 9,72 V
IDN1 IDN2 IDP1 IDP2	6.40MA 15.0MA -1.99MA -4.49MA	6.15MA 13.8MA -2,03MA -4,57MA	5.75MA 12.1MA ~1.94MA ~4.33MA	5,75MA 12,4MA +2,20MA +4,56MA
IOZ1 IOZ2 IOZ3 IOZ4	1,41UA 1,40UA 1,39UA 1,39UA	1.55UA 1.55UA 1.54UA 1.53UA	1.61UA 1.61UA 1.61UA 1.61UA	1,47UA 1,47UA 1,46UA 1,47UA
1025 1026 1027 1028	1.40UA 1.41UA 1.41UA 1.40UA	1,56UA 1,55UA 1,54UA 1,54UA	1.63UA 1.63UA 1.62UA 1.61UA	1,50UA 1,48UA 1,47UA 1,48UA
ILDP	70.0UA			
IL: IL2 IL3 IL4	-160.HA -195.UA -165.UA			

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RCA CDP1822SD 256 X 4	CMOS STATI	C RAM 31	AUG 78 TEMP:	25 C SN:
				. 05 .0
			PAGF	1 OF 10
PASSED GALPAT (NIDE LI	MITS) VCC=	: CAV		
PASSED GALPAT (TIGHT LI				
PASSED GALPAT (TIGHT LI				
		-		
PASSED DATA RETENTION TE	\$7			
			•	r
	vcc =	4.5V	5.0V	10.0V
				-nt-n.
ADDRESS ACCESS TIME	(TAA)	285.N	235'N	96 ON
DATA SETUP TIME	(TDS)	24, ØN	20,0N	8.000
DATA HOLD TIME	(TOH)	14.0N	12.an	12.0N
ADDRESS SETUP TIME	(TAS1)	16.0N	12.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	134.N	112.N	54.0N
ADDRESS HOLD TIME	(TAH)	-18,0N	-14. MN	-4.00N
WRITE PULSE WINTH	(TWP)	74 . ON	65° NN	36.0N
	-		, ,	
CS1 SETUP TIME	(TCSS1)	180.N	152°N	74 0N
CSP SETUP TIME	(TCSS2)	174.N	150.N	72,0N
CS1 HOLD TIME	(TCSH1)	36,0N	32.MN	22,0N
CSS HOLD TIME	(TCSH2)	38.ØN	34,0N	55,0N
MITMIT COSTUS STAN AGE	/*****	370 W	224 1	4.0.5 N
OUTPUT ACTIVE FROM CS1	(TDOA1)	270 N	224, N	102.N
OUTPUT ACTIVE FROM CS2	(SADOT)	266.N 56.ØN	222.N	98,0N 98,0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	भाख • व द	50.0N	ឌីជឺ " ស៊ីស
OUTPUT HOLD FROM CS1	(троні)	156.N	122,N	32,0N
OUTPUT HOLD FROM CS2	(TDOH2)	150 N	118,N	32,0N
OUTPUT HOLD FROM MRD	(TDOH3)	140.N	116 N	34, ØN
OUTPUT HOLD FROM MUR	(TPDH)	138 N	112,N	36.0N
READ CYCLE TIME	(TRC)	296.N	248 N	128.N
WRITE CYCLE TIME	(TWG)	264.N	232.N	iae.N

	IIL	IIH	VICI	AICS
AØ	-2,40NA	2,10NA	3.07 V	-3,05 V
A 1	#2.10NA	1,90NA	3.08 V	e3,11 V
A2	⇒3. 00NA	1,80NA	3.10 V	-3,12 V
43	#2.00NA	5.50NA	3,07 V	-3,11 V
A 4)	-1.90NA	1,50NA	3.11 V	-3,13 V
A5	-2.30NA	2,00NA	3.04 V	-3,08 V
A 6	-2.40NA	1.8PNA	3.04 V	#3,08 V
A 7	-2,20NA	A/NN.S	3_04 V	-3.09 V
CS1	-1.90NA	1,90NA	3.09 V	-3/11 V
CS2	-1.90NA	2,00NA	3.13 V	-3,10 V
MWR	₩2.10NA	A'SONA	3.06 V	#3,08 V
MRD	⇒1.80NA	2.70NA	3.08 V	#3,11 V
DIØ	-2.50NA	2.60NA	3.15 V	-3,09 V
011	-2,10NA	2,10NA	3.13 V	÷3,09 V
DIS	-2.60NA	1.90NA	3,14 V	-3.09 V
013	-270.NA	2.10NA	3.14 V	-3.09 V

RCA	CDP1822\$D	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMPi	25 C	SN:	29 29
nun	POLISSEN	EDO A 4 DOO	OTALTE MAIL	11 MOD 10	1 In 1945 B	E 7 B	G1* \$	Her d
					PAGE	2 OF	10	: g. a
	000	DO1	naz	003				1.2
	WO FE	boî	NAE	003				
VOLI	120.MV	125,MV	135,MV	130° MV				25
VOL2	120.MV	125.MV	140 MY	140 MV				
VOH1	4 84 V	4 84 V	4,84 V	4,84 V				
VOHE	9,77 V	9.78 V	9.77 V	9,77 V				÷ . 3
		t	į					5 · ii
IDN1	6.05MA	5.90MA	5.60MA	5.60MA				
IDNS	15.8MA	15.0MA	13.7MA	13,9MA				• :
IOP1	≈2 ,43MΛ	₩2°41ħV	-2.37MA	-2,41MA				₹ 21
1055	-5.53MA	+5.55MA	-5.36MA	-5,55MA				
¥074	E4 05'4	CC ONA	49 4NA	46 7NA				
TOZ1	51.0NA	SØ. BNA	49,4NA	46.3NA				W ₁ (2)
	47.8NA	53.8NA	45.7NA	49.5NA				
1073	54.7NA	45.6NA	51,4NA	45,0NA				* - .
1074	52.7NA	46,1NA	51.6NA	43.8NA				. 2
1025	47.5NA	/ 53.6NA	47,0NA	52.8NA				
1026	48 8NA	53.7NA	44 000	51.4NA				98 S
IUZ7	47.9NA	53.2NA	46 ØNA 46 NA	51.9NA				11 2 2
1028	47.9NA	53,3NA	45.5NA	51.2NA				5.
1070	41#3147	D 3 * DAW	AMC#CH	BI#CHH				طع اومو
ILDP	*5.00UA							7.0
IL1	-20.0HA							* :
1 - 1	TEVIA WITH							

IL2 IL3 IL4

-45.0UA -30.0UA -50.0UA

PAGE 3 OF 10

PASSED GALPAT	(WIDE LIMITS)	VCC=10V	REPRODUCIBILITY OF THE
PASSED GALPAT	(TIGHT LIMITS)	VCC=10V	ORIGINAL PAGE IS POOR
PASSED GALPAT	(TIGHT LIMITS)	VCC=5V	Q19101111111111111111111111111111111111

r				- * -	lata.
		VC.	= 4.5V	5.0V	10.0V
ADDRESS	ACCESS TIME	(TAA)	295.N	230', N	85.0N
	THP TIME	(TDS)	28,0N	22.WN	8.00N
	OLD TIME	(TDH)	15.0N	10.0N	12.00
ANDRES	CETUS TIME	/ T A C 4 3	16.0N	12.9N	4.00N
	SETUP TIME	(TAS1)		106.N	48.0N
	S SETUP TIME	(TAS2) (TAH)	134 N	-14.0N	-4.00N
	3 HOLD TIME PULSE WIDTH	(TWP)	-18.0N 76.0N	68.0N	34.0N
METTE:	Orgc Miniu	(TWF)	A O W SAIA		74.00
CS1 SE	TUP TIME	(TCSS1)	172.N	144.N	68,0N
CS2 SE	ETUP TIME	(TCSS2)	168.N	145 N	66,0N
CS1 HC	DLD TIME	(TCSH1)	38.ØN	30.0N	22,0N
C\$2 HC	THE TIME	(TCSH2)	38,ØN	34. NN	50,0N
питент	ACTIVE FROM CS	31 (TDOA1)	266.N	216 N	94, ON
	ACTIVE FROM CS		266 N	214 N	90,0N
	ACTIVE FROM ME		ระโด้ท	46. AN	26. ØN
9011 (11	WOLLAR LINGS IN	(0.0043)	J. 20 "		
OUTPUT	HOLD FROM CS1	(TDOH1)	148 . N	114 N	30,0N
OUTPUT	HOLD FROM CS2	(SHOOT)	144.N	112°N	30,0N
OUTPUT	HOLD FROM MRD	(TDOH3)	136.N	116,N	32,0N
DUTPUT	HOLD FROM MWR	(TPDH)	136.N	110,N	32.0N
	YCLE TIME	(TRC)	280,N	232,N	120.N
WRITE (CYCLF TIME	(TWC)	240 N	208.N	112.N
	714	IIH	VIC1	VICE	
AØ	=500.PA	400, PA	3.15 V	+3,13 V	
A1	-500 FA	300 PA	3.16 V	-3,18 V	
2 A	-900.PA	200 PA	3.17 V	-3,18 V	
A 3	-300.PA	500.PA	3.15 V	ต่ิ∄ี่มีR V	
A4	_#@@ ©A	200 PA	7 10 V	•3,19 V	
A5	=400.PA =400.PA	400.PA	3.18 V 3.13 V	-3,14 V	
A6	=500.PA	300 _p PA	3,13 V	+3,15 V	
A 7	=400 PA	300 PA	3.13 V	=3.16 V	
- ·	a a to to a to to	M 3 W th W	<i>⊒ • (22 ∨</i>		
CSi	-400.PA	400.PA	3,17 V	-3,17 V	
cs2	-400 PA	400 PA	3.21 V	#3,16 V #3,15 V #3,17 V	
MWR	-400.PA	490,PA	3.14 V	+3,15 V	
MRD	m300.PA	700.PA	3.16 V	≈3.17 V	
DIO	-500.PA	500.PA	3.23 V	-3,16 V	
DII	-400.PA	300.PA	3.20 V	=3,16 V	
DIS	≈ 500.РА	400 PA	3.22 V	#3,16 V #3,16 V	
013	-154 NA	400 PA	3.22 V	-3.15 V	
			•	*	

RCA	CDP1822SD	256	X	4	CMOS	STATIC	RAM	31	AUG	78	TEMP:	20	C	SN:	59
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PAGE	4	OF	10
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	ካበብ	po1	005	003
VOL 1	110.MV	115.HV	120.MV	120, MV
AOF 5	105.MV	110.MV	125.MV	1 PO LMV
VOH1	4.86 V	4 86 V	4.86 V	4,86 V
SHOV	9.81 V	9 81 V	9.80 V	9 81 V
IDN1	6.65MA	6.45MA	6.20MA	6,20MA
IDNS	17.8MA	16.9MA	15.5MA	15.7MA
IUPi	-2,86MA	-2,84MA	≈2.81MA	-2,84MA
IDP2	₩6 _₩ 53MA	-6.55MA	-6.37MA	=6.58MA
IUZ1	10.9NA	4,20KA	10.5NA	3'.30NA
1072	7.60NA	6.60NA	7.80NA	4 ៉ូ 5 ^{រា} NA
1073	7.1004	4405.8	4.9UNA	8 40NA
1024	10.5NA	4.90NA	8.10NA	5.20NA
1025	5.60NA	8,40NA	5.80NA	7,20NA
1076	5.90NA	ยโรดกล	5.80NA	6,5MNA
1027	5.9UNA	7.90NA	6.00NA	6,90NA
1028	5.90NA	8.20NA	6. ØUNA	6.2MNA
ILDP	≈1.49UA			
IL1	∞15 _≠ ØUA			
ILS	-40.0UA			
IL3	-25,ØUA			
IL4	-40 WHA			

PASSED	GALPAT	(MIDE	LIMITS)	VCC=10V
PASSED	GALPAT	ไหลเไ)	LIMITS)	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS)	VCC=5V

PASSED DATA RETENTION TEST

	ycc	= 4.5V	5,0v	10.0V
ADDRESS ACCESS TIME	(TAA)	295.N	220.N	80'.0N
DATA SETUP TIME	(TDS)	34,0N	24.0N	8.00N
DATA HOLD TIME	(HOT)	10.0N	10.6N	10.0N
	4 10.13	101011	To. White	10.50
ADDRESS SETUP TIME	(TAS1)	12,0N	8.00N	4.99N
ADDRESS SETUP TIME	(TAS2)	134.N	104 N	44. ØN
AUDRESS HOLD TIME	(HAH)	-18,ØN	-14 ON	-4.00N
WRITE PULSE WIDTH	(TWP)	84 <u>.</u> ØN	70.0N	35.0M
			•	ŧ
CS1 SETUP TIME	(TCSS1)	170.N	142,N	64,0N
CS2 SETUP TIME	(TCSS2)	170.N	138.N	62,0N
CS1 HOLD TIME	(TCSH1)	44,0N	32,0N	20,0N
CSS HOLD TIME	(TCSH2)	48.0N	38.9N	20,0N
DUTPUT ACTIVE FROM CS1	CTD0 443	220 11	2401	oa'av
OUTPUT ACTIVE FROM CS2	(TDOA1)	278.N	214'N	90,0N
OUTPHT ACTIVE FROM MRD	(SACOT)	276.N	212.N	88 ØN
OUTCOL ACTIVE PROPERTY	(TDOA3)	50.0N	42.AN	24.0N
OUTPUT HOLD FROM CS1	(TDOH1)	142.N	108 N	26, 0N
OUTPUT HOLD FROM CS2	(SHOOT)	138.N	104 N	26,00
OUTPUT HOLD FROM MRD	(TDOH3)	136.N	114,N	30,0N
OUTPUT HOLD FROM MUR	(TPDH)	134 N	110,1	32.0N
READ CYCLE TIME	(TRC)	272.N	216 N	112.N
WRITE CYCLE TIME	(TWC)	264.N	208.N	104.N
and the second second	()	E0.04	E e. O a . A	1 57 9 14
IIr IIH		VICi	VIC5	
A0 =100,PA 100	* P.A. ·	3.24 V	-3,21 V	
A1 #100.PA 100	р. и Р л	3.24 V	#3,56 V	
A2 -300,PA 100		3,26 V	±3,27 V	
A3 -100.PA 100		3.24 V	#3,26 V #3,27 V #3,27 V.	
Ca artholic a tank	# (A	7 6 5 A	wastr v.	
A4 =100_PA 100	₌₽A	3.27 V	=3,28 V	
A5 -100.PA 100	PA	3.21 V	#3,23 V	
	PA	3.21 V	-3,24 V	
A7 +100.PA 100	.PA	3.21 V	-3,24 V -3,25 V	
604 .400 m	' m »			
CS1 =100.PA 100		3.26 V	-3,26 V	
CS2 ~100.PA 100		3.30 V	-3,25 V	
MWR =100,PA 100	r H A	3.24 V	-3,24 V	
MRD -100.PA 100	. P A	3.25 V	=3,26 V	
DIO -100_PA 100	- PA	3,32 V	#3,25 V	
DI1 -100,PA 100		3 29 V	#3,25 V	
DI2 -100.PA 100	ΡΔ	3.31 V	3,24 V	
DI3 =96.1NA 100		3.31 V	=3,24 V	
TOO TOOLS	.		~~* G7 V	
		TO 200	•	

REA	088581400	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMPI	#55 C	SNI	59
					PAGF	6 OF	10	
	noø	DO1	500	003				
240v 140v 140v 110v	105.MV 95.0MV 4.88 V 9.84 V	105.MV 100.MV 4.88 V 9.84 V	110 mV 110 mV 4 88 V 9 84 V	110,MV 110,MV 4,88 V 9,84 V				
ION1 ION2 IOP2 IOP2	7.15MA 19.6MA -3.27MA -7.49MA	6 99MA 18.7MA +3.28MA +7.57MA	6.65MA 17.2MA -3.25MA -7.35MA	6.65MA 17.4MA -3,29MA -7.69MA				
1071 1022 1023 1024	3.10NA -300.PA 6.10NA 5.00NA	2,00NA 5.50NA -500.PA -900.PA	3.20NA -50M.PA 4.40NA 4.80NA	500.PA 4.20NA +100.PA -1.20NA				
1025 1026 1027 1028	-400.PA -100.PA -100.PA 500.PA	4,90	-1.20NA -1.20NA -900.PA -1.10NA	5,40NA 5,00NA 5,00NA 4.80NA				
ILDP	-15.0UA							
IL1 IL2 IL3 IL4	-15,0UA -35,0UA -25,0UA -40,0UA							

RCA CDP1822SD 256 X 4 CHOS STATIC RAM 31 AUG 78 TEMP: 85 C SN: 29

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PASSED GALPAT (WIDE PASSED GALPAT (TIGHT PASSED DATA RETENTION	T LIMITS) VC T LIMITS) VC	C=10V C=10V C=5V	REPRODUCIBIL ORIGINAL PA	TYYOFF THE
	VCC	= 4.5V	5'.@V	10.0v
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA) (TDS) (TDH)	280	235.N 20.0N 14.0N	100.N 8.00N 14.0N
ADDRESS SETUP TIME AUDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WIDTH	(TAS1) (TAS2) (TAH) (TWP)	8.00N 136.N -18.0N -86.0N	8.00N 118.N -14.0N 76.0N	42.0N 42.0N 42.0N
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS1) (TCSS2) (TCSH1) (TCSH2)	186.N 182.N 50.0N 54.0N	160,N 158.N 44.MN 48.MN	82,0N 78,0N 28,0N 28.0N
OUTPUT ACTIVE FROM COUTPUT ACTIVE FROM COUTPUT ACTIVE FROM MI	S2 (TDOA2)	268 N 264 N 60 0 N	232,1 228,N 52.0N	112.N 110.N 30.0N
OUTPUT HOLD FROM CS: OUTPUT HOLD FROM NRD OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME		154.N	126'N 124'N 118'N 114'N 256'N 224'N	36,0N 36,0N 38,0N 38.0N 136.N
IIL	IIH	VIC1	v1C5	
A0 =22.9NA A1 =23.2NA A2 =23.9NA A3 =23.0NA	23,1NA - 22,1NA 22,8NA 22,4NA	3.03 V 3.04 V 3.06 V 3.03 V	#3.01 V #3.06 V #3.08 V #3.08 V	
A4 #22,1NA A5 #24,1NA A6 #23,6NA A7 #24.2NA	20.4NA 22.3NA 22.1NA 21.6NA	3.08 V 3.00 V 3.00 V	=3,10 V 0, =3,03 V =3,04 V =3,05 V	EPRODUCIBILITY OF THE
CS1 =21,8NA CS2 =21.8NA MWR =22,0NA MRD =22.3NA	21.2NA 22.3NA 22.5NA 24.8NA	3.05 V 3.10 V 3.02 V 3.04 V	-3,06 V -3,06 V -3,04 V -3,07 V	OF THE
DIO =24,1NA DI1 =22,6NA DI2 =23,4NA DI3 =509,NA	24,6NA 22.1NA 21.6NA 22.1NA	3.11 V 3.09 V 3.10 V 3.11 V	3,05 V 3,05 V 3,05 V 3,04 V	

RCA	CDP18225D	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMPS	85 C S
					PAGE	8 QF 10
	מממ	t 0.0	Doa	003		
VOL 1	140.MV	145.MV	155.MV	150, MV		
VOLE	140.MV	150.MV	165.MV	160. MV		
VOH:	4.81 V	4,81 V	4.80 V	4,81 V		
AOHS	9,73 V	9.74 V	9.72 V	9.73 V		
ION1	5.30MA	5.15MA	4.90MA	4.90MA		
10/15	13.6MA	12.8MA	11.7MA	_11.8MA		
IDP1	-2.06MA	-2.05MA	#2.01MA	-2,05MA		
INPS	∞4.70MA	-4.73MA	-4.57MA	-4.73MA		
TOZ1	505.NA	492 . NA	492.NA	468, NA		
1025	506.NA	484.NA	493.NA	472,NA		
1073	499.NA	486 "NA	496.NA	471, NA		
1024	505.NA	483 . NA	490.NA	476.NA		
1025	508.NA	493,NA	509.NA	491 .NA		
IC26	510.NA	497.NA	489.NA	485.NA		
IUZ7	501.NA	493 "NA	496 .NA	474, NA		
1028	513.NA	488.NA	493.NA	481 NA		
ILDP	6.00UA					
11.1	=40,0UA					
IL2	-70.0UA					
IL3	-55,0UA					
IL4	-75.0UA					
T per al						

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V/2

2011

SN:

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PASSED	GALPAT	(WIDE	LIMITS)	VCC=1ØV
PASSED	GALPAT	(TIGHT	LIMITS)	VCC#1@V
PASSED	GALPAT	(TİGHT	LIMITS)	VCC=5V

PASSED DATA RETENTION TEST

	VCC	C = 4.5V	5'.0V	10'.0V
ADDRESS ACCESS TIM DATA SETUP TIME DATA HOLD TIME	E (TAA) (TDS) (TDH)	285.N 26,0N 18.0N	245'N 22.0N 18.0N	110.N 10.0N 16.0N
ADDRESS SETUP TIME ADDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WIDTH	(TAS1) (TAS2) (TAH) (TWP)	4.00N 140.N -18.0N 92.0N	4'.00K 126'.N +16.0N 82.0N	4.00n 68.0n -4.00n 46.0n
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS1) (TCSS2) (TCSH1) (TCSH2)	198 N 194 N 54 ON 58 ON	172'N 168'N 48', an 52', an	88,0N N0,68 N0,0E N0,0E
OUTPUT ACTIVE FROM OUTPUT ACTIVE FROM OUTPUT ACTIVE FROM	CS2 (TDOA2)	284.N 280.N 64.0N	246'N 242'N 56'N	124.N 127.N 32.0N
OUTPUT HOLD FROM COUTPUT HOLD FROM MODITPUT HOLD FROM MODITPUT HOLD FROM MOREAD CYCLE TIME WRITE CYCLE TIME	sa (TDOH2)	160N 156N 140N 140N 312N 264N	130, K 176, N 118, N 116, N 264, N 240, N	40,8N 40,0N 38,0N 38.0N 144.N
III	IIH	VIC1	VICE	
A0 #125,NA A1 #127,NA A2 #125,NA A3 #124,NA	121.NA 123.NA 121.NA 118.NA	3.03 V 3.05 V 3.02 V	=3,00 V =3,05 V =3,08 V =3,07 V	
A4 =120.NA A5 =126.NA A6 =127.NA A7 =129.NA	113, NA 120, NA 120, NA 118. NA	3.06 V 2.99 V 2.99 V 2.99 V	-3'09 V -3'02 V -3'03 V -3'04 V	
CS1 #123.NA CS2 #120.NA MWR #119.NA MRD #122.NA	114,NA 122,NA 116,NA 121.NA	3,04 V 3,09 V 3,01 V 3,02 V	93,05 V 93,05 V 93,03 V 93,06 V	
DIØ #125.NA DI1 #121.NA DI2 #122.NA DI3 #873.NA	124.82 120.Na 117.Na 116.Na	3.10 V 3.09 V 3.10 V 3.10 V	=3,04 V =3,04 V =3,04 V	

RCA	CDP18228D	256 X 4	CMOS	STATIC	RAM	31	AUG	78	TEMP	125	C	SN:	29

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	ው የ	001	poz	003
VOL2 VOH2 VOH2	155.MV 155.MV 4.78 V 9.70 V	160 MV 165 MV 4,78 V 9,70 V	170.MV 185.MV 4.78 V 9.69 V	170'.MV 180'.MV 4'.78 V 9'.70 V
ION1 IDN2 IOP1 IOP2	4.80MA 12.2MA =1.86MA =4.24MA	4.65MA 11.4MA +1.86MA +4.25MA	4.45MA 10.4MA =1.81MA =4.09MA	4.45MA 10.6MA -1.84MA -4.27MA
1071 1072 1073 1074	2.01UA 2.01UA 2.00UA 1.99UA	1,97UA 1,96UA 1,96UA 1,96UA	1,94UA 1,95UA 1,95UA 1,95UA	1,900A 1,890A 1,900A 1,900A
1025 1026 1027 1028	5.02UA VUED.5 VUED.5	1,99UA 1,99UA 1,98UA 1,97UA	2.00UA 1.96UA 1.96UA 1.96UA	1,96UA 1,92UA 1,92UA 1,92UA
ILDP	25.MUA			
TL1 IL2 IL3 IL4	=115 eUA =160 eUA =140 eUA =150 eUA			

PAGE 1 OF 10

				PAG	F 1 OF 10
		LIMITS) T LIMITS)	VCC=10V VCC=10V	•	
	- ,	T LIMITS)	VCC=5V	REPRODUCIBILIT	Y OF THE
PASSED	DATA RETENTIO	N TEST		ORIGINAL PAGE	IS POOR,
			VCC = 4.5V	5 , øv	10.0V
	S ACCESS TIME	(TAA)	235.N	2ØØ, N	85,0N
	ETUP TIME OLD TIME	(TDS) (TDH)	22, ØN	18,0N	8.60N
		Cluns	10.0N	10.0N	10.0N
	S SETUP TIME	(TAS1		10.0N	4.90N
	S SETUP TIME S HOLD TIME	(TAS2 (TAH)		_96,0N =14,0N	48.0N
	Pulse winth	(TWP)	∺16,0N 70.0N	60.AN	=4,00N 36.0N
004 00	Callo erus			•	
	ETUP TIME ETUP TIME	(TCSS (TCSS)		140'N 284'N	70 ON
	PLO TIME	(TCSH		34,0N	70,0N 22,0N
CSS H	DLD TIME	(TCSH		28.0N	16.0N
OUTPUT	ACTIVE FROM C	S1 (TDOA		194' _F N	90,0N
		SE (TOOA)		196.N	94,0N
	ACTIVE FROM ME			44.70	26.0N
OUTPUT	HOLD FROM CS:	CTDOH	i) i42,N	110 N	28,0N
OUTPUT	HOLD FROM CS2	CTDON		114 _p N	32,0N
	HOLD FROM MRD	(TDOH:	3) 136.N	114 N	34,0N
	HOLD FROM MWR	(TPOH)		110,N	34,0N
	CYCLE TIME	(TRC) (TWC)	256.N 224.N	216 N 192 N	120.N 112.N
	IIL	IIH	VIC1	VIC5	
AØ	- 4 7 (2 N A	4' 00014			
Al	∞1,70NA ∞1,40NA	1,90NA 1,90NA	2,96 V	#2,95 V #3,00 V	
A2	-2.10NA	1,40NA	3.01 V	⇔3,00 V ⊕3,04 V	
A3	-1.90NA	1.50NA	3.01 V	≖3 Ø6 V	
A 4	-1.60NA	1,50NA	3.05 V	#3,10 V	
A5	-1.46NA	1,40NA	2.94 V	₩2,98 V	
A6	-2.00NA	1,40NA	2.95 V	-2,95 V	
A 7	-1.40NA	1.60NA	2.95 V	⇔2 97 V	
CS1	=1.30NA	1,60NA	3,00 V	-3,02 V	
CS2 MWR	-1.70NA -1.80NA	1,70NA	5.01 V	ლ4,9₽ V	
MRD	#1.40NA	1,30NA 1.30NA	2,99 V 3.00 V	=3.01 V ≈3.03 V	
	-				
DIØ DI1	-1,70NA -1,20NA	1,30NA 1,40NA	3.41 V	92,97 V	
015	-1,80NA	5 2 2 0 N A	3.09 V	-2,96 V -3,02 V	
013	#1.50NA	1.60NA	3.06 V	-3.00 V	

11.50

RCA	CDP1822SD	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP	25 C SN:
					PAGE	2 OF 10
	000	001	noż	003		
VQL1	95 0MV	100.MV	110.MV	105, MV		
VOLE	105.MV	110.MV	125.MV	1,25 MV		
VOH1	4.86 V	4.85 V	4.85 V	4,86 V		
AnHS	9.78 V	9.78 V	9.78 V	9.79 V		
IDNI	7.60MA	7 . 40MA	6.75MA	6.90MA		
IDNZ	15.3MA	17.2MA	15.1MA	15.5MA		
IDP1	-2,65MA	-2.65MA	-2.57MA	-2,65MA		
IDP2	-5.79MA	-5.83MA	-5_61MA	-5.85MA		
IOZi	10,9NA	16.0NA	11,4NA	15.2NA		
IOZZ	10,3NA	16.6NA	10,1NA	16.7NA		
1023	16,2NA	9.90NA	17,0NA	9.50NA		
1074	13,5NA	12.1NA	14.7NA	1M. BNA		
1025	12.0NA	14.8NA	11,3NA	15,6NA		
1026	11.6NA	14.8NA	11,3NA	15.7NA		
1027	11.7NA	15.1NA	10,7NA	15.6NA		
1028	11.3NA	14.7NA	11. (NA	15,9NA		
ILOP	-20.0UA					
ILi	-20.WUA					
ILZ	~20.0UA					
IL3	-20.0UA					
11.4	-15.0UA					
•••	7 m m - / - 10					

PAGE 3 OF 10

PASSED	GALPAT	(MIDE	LIMITS)	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS)	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS)	VCC=5V

PASSED DATA RETENTION TEST

To the second of

	VCC	= 4 ₈ 5V	5 . 0v	10.0V
ADDRESS ACCESS TIME	(TAA)	235.N	190 N	75.0N
DATA SETUP TIME	(TDS)	24,0N	Sù DN	8.00N
DATA HOLD TIME	(HOH)	8.000	8.00N	10.0N
ADDRESS SETUP TIME	(TAS1)	16.0N	12.0N	4 . 00 N
ADDRESS SETUP TIME	(TASE)	119 N	92.AN	42.2N
ADDRESS HOLD TIME	(TAH)	≖16,0N 70,0N	∞12,7N = 2 7N	42.0N
WRITE PULSE WINTH	(TWP)	/ W P M	58.0N	
CS1 SETUP TIME	(TESS1)	154.N	130, N	62, ØN
CS2 SETUP TIME	(TCSS2)	152.N	130 N	62,0N
CS1 HOLD TIME	(TCSH1)	36,0N	30 an	20,0N 18.0N
CS2 HOLD TIME	(TCSH2)	36,0N	30 . ON	
OUTPUT ACTIVE FROM CS1	(TDOA1)	222°N	184, N	88, ØN
OUTPUT ACTIVE FROM CS2	(SACCT)	555"N	182.N	86, ØN
OUTPUT ACTIVE FROM MRD	(TDOA3)	46 . ØN	40. AN	24,0N
OUTPUT HOLD FROM CS1	(TOOH1)	132.N	102,N	24°, 0N
BUTPUT HOLD FROM CS2	(SHOOT)	132,N	105"	26, ØN
OUTPUT HOLD FROM MRD	(TDOH3)	132.N	112 N	30,0N
OUTPUT HOLD FROM MUR	(TPDH)	128.N	106,N	32.0N
READ CYCLE TIME WRITE CYCLE TIME	(TRC) (TWC)	232.N 238.N	200,N 176.N	112.N 104.N
MATE CIOCE I CHE	(i we j	EXIO .	1,024	204811
IIL III	4	VIC1	AICS	
AØ =300.PA 300	a, PA	3.02 V	≖3,00 V	
	a⊊PA	3.04 V	•3,05 V	
	D.PA	3.06 V	-3.09 V	
A3 -400.PA 200	ā.PA	3.96 V	-3.11 V	
A4 =200,P4 200	2', PA	3.11 V	=3,13 V	
A5 #200.PA 200	D,PA	3.00 V	≕3.03 V	4
A6 -300.PA 200	0, PA	3.01 V	-3,01 V	
A7 #200.PA 300	2.PA	3.01 V	-3.02 V	
CS1 =100.PA 400	Ø a PA	3.05 V	=3,08 V =3,60 V =3,06 V	
	η.PA	3,60 V	-3,60 V	
	7, PA	3,04 V	93,06 V	
MRD =200.PA 20	N.PA	3,05 V	=3.08 V	
DI0 -200.PA 200	n'₊PA	3.07 V	.3,02 V	
	D.PA	3,06 V	e3,01 V	
	Z,PA	3.14 V	±3,08 V	
DI3 =200,PA 300	D.PA	3.12 V	≈3 ,05 V	

064	COP18225D	956	V 11	CMOC	CTATTO	D AM	71	AUG 7	o T	'EMB	-26	r	SNE	30
MLA	たいしょりにゅうひ	435	X 4	しいいる	DIVITE	KAN	- J	AUU /	0 1	Ent.	4. C. C.	U	Q IV P	J. 10.

PAGE 4 0F 10

	DOW	100	002	003
VOL 1	AS MMV	85.0MV 95.0MV	95.0MV 110.MV	90.0MV
AOL S	90 0 MV			105 MV
VOH1	4.88 V	4,88 V	4.88 V	4 88 V
VOH2	9.82 V	9.85 V	9.81 V	9,82 V
ION1	8.70MA	8,50MA	7.80MA	7.90MA
IDNS	21.2MA	19.9MA	17.5MA	18.0HA
IDP1	#3.15MA	-5,15MA	-3.11MA	=3,16MA
IDP2	-6.88MA	-6.92MA	₽6.74MA	-6.97MA
w = · •	• • • • • • • • • • • • • • • • • • • •			
IOZi	6.50NA	-600.PA	6,30NA	-800 PA
IOZZ	3.00NA	1.80NA	3.30NA	500.PA
1023	2 4MNA	3.30NA	800 PA	4 DONA
IOZ4	6.00NA	-100.PA	4.60NA	500 PA
	•			
1075	300.PA	4 40NA	600.PA	3,80NA
1076	300.PA	4 <u>9</u> 0NA	500.PA	3,60NA
1027	300.PA	4.60NA	500.PA	3,60NA 3,90NA
IOZ8	100.PA	5.20NA	300.PA	3,60NA
W == W	* " · •		•	- - -
ILOP	#5.80UV			
ILi	+20,0UA			
ĭĽŠ	-15.0UA			
IL3	≈15.0UA			
IL4	-10.0UA			
⊕ #= -7	7 to 8 to 14			

RÇA	CDP1822SD	256 X 4	CMOS	STATIC R	RAM 31	AUG	78	TEMP	#55 C	SN:	30
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PAGE 5 OF 10

PASSED GALPAT (TIGHT	r LIMITS) VC	C=10V C=10V C=5V	REPRODUCIBI ORIGINAL PA	
PASSED DATA RETENTION	N TEST			·
	vcc	= 4,5V	5,0V	10.0V
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA) (TDS) (TDH)	225.N 28.0N 6.00N	180 ¹ N 22.0K 8.00N	70', 0N 8, 00N 8, 00N
ADDRESS SETUP TIME ADDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WIDTH	(TAS1) (TAS2) (TAH) (TWP)	14.0N 106.N -16.0N 70.0N	10,00 88,00 *12.00 58.00	4.00N 38.0N -2.00N 30.0N
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS1) (TCSS2) (TCSH1) (TCSH2)	146 N 146 N 36 DN 38 ON	176, N 124. N 32. ØN 34. ØN	58,0N 58,0N 16,0N
OUTPUT ACTIVE FROM COUTPUT ACTIVE FROM MO	(SAODT) SE	216.N 216.N 42.ØN	174, N 172, N 36, MN	84, ØN 82, ØN 22. ØN
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM CS2 OUTPUT HOLD FROM MWR OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH1) (TDOH2) (TDOH3) (TPOH) (TRC) (TWC)	126 N 126 N 132 N 128 N 216 N 192 N	94.0N 94.0N 110.N 104.N 184.N 168.N	22,0N 24,0N 30,0N 300,0 104,0N
IIL	IIH	VIC1	VIC2	
A0 = 100.PA A1 = 100.PA A2 = 100.PA A3 = 100.PA	100,PA 100,PA 0,00 A 100,PA	3.08 V 3.11 V 3.01 V 3.12 V	-3,07 V -3,12 V -3,14 V -3,16 V	
A4 =100.PA A5 0.00 A A6 =100.PA A7 =100.PA	0.00 A 100.PA 100.PA 100.PA	3.15 V 3.06 V 3.08 V 3.08 V	13/19 V 3/10 V 3/08 V 3/09 V	
CS1 0.00 A CS2 +100.PA MWR -100.PA MRD +100.PA	100,PA 100,PA 100,PA 0.00 A	3,12 V 3,69 V 3,10 V 3,12 V	-3,13 V -3,68 V -3,12 V -3,13 V	
DIO =100.PA DI1 0.00 A DI2 =100.PA DI3 0.00 A	0.00 A 100,PA 200,PA 100.PA	3.13 V 3.12 V 3.20 V 3.17 V	=3,09 V =3,08 V =3,13 V =3,12 V	
		B-295		

RCA	CDP1822SD	256 X	4	CMOS	STATIC	RAM	31	AUG	78	TEMPi	-55	C	SN:	30
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	DOØ	100	200	D03	
VOL1 VOL2 VOH2	75.0MV 80.0MV 4.89 V 9.85 V	75.0MV 85.0MV 4,89 V 9.84 V	85',0MV 95',0MV 4,39 V 9,84 V	85,0MV 95,0MV 4,89 V 9,85 V	
IDN1 IDN2 IDP1 IDP2	9.70MA 23.7MA -3.66MA -7.95MA	9.50MA 22.4MA -3.70MA -8.05MA	8.70MA 19.8MA =3.61MA =7.80MA	8'.80MA _20'.3MA =3'.71MA =8.10MA	
1021 1022 1023 1024	-200.PA 2.90NA 700.PA -1.60NA	3.80NA 400.PA 1.80NA 5.20NA	-1.50NA 1.60NA 1.20NA -1.80NA	4,20NA 1,20NA 500,PA 4,10NA	
1025 1026 1027 1028	5.50NA 5.20NA 5.50NA 5.30NA	-1.60NA -1.60NA -1.70NA -1.70NA	3.90NA 4.30NA 4.30NA 4.60NA	=1,20NA =1,20NA =1,30NA =1,40NA	
ILDP	-1.20UA				
IL1 IL2 IL3 IL4	-20.0UA -15.0UA -15.0UA -10.0UA				

RÇA	CDP1822SD	256 X 4	CMOS ST	ATIC RAM	3 i	AUG 78	TEMP:	85 C	SN:	30
							PARE	7 OF 1	. P	

PASSED	GALPAT	(WIDE	LIMITS)	VCC=10V
PASSED	GALPAT	CTIGHT	LIMITS)	VCC=10V
PASSED	GALPAT	(TIGHT	(.IMITS)	VCC=5V

PASSED DATA RETENTION TEST

	VCC	= 4.5V	5 . øv	10.0v
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA) (TDS) (TDH)	240.N 24.0N 12.0N	210'.N 20.0N 12.0N	95,0N 8.0N 12.0N
ADDRESS SETUP TIME ADDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WIDTH	(TASL) (TASZ) (TAH) (TWT)	8.00N 120.N -18.0N 82.0N	8.00N 104.N -14.0N 72.0N	4.00N 54.0N =4.00N 42.0N
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(1882T) (5882T) (1882T) (1882T)	174.N 170.N 52.ØN 54.ØN	150', N 148', N 46', MN 48', MN	78,0N 76,0N 26,0N 26.0N
OUTPUT ACTIVE FROM CS: OUTPUT ACTIVE FROM CS: OUTPUT ACTIVE FROM MRD	(SA00T)	240.N 236.N 56.0N	208'N 508'N	104,N 102,N 30.0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH1) (TDOH2) (TDOH3) (TPOH) (TRC) (TWC)	148 N 144 N 138 N 134 N 264 N 252 N	116, N 114, N 118, N 112, N 232, N 208, N	34,0N 34,0N 36,0N 36.0N 128,N
	IIH	Alct	VICE	- y
A1 -20.7NA 3	22.5NA 22.9NA 21.3NA 21.8NA	2.94 V 2.97 V 2.98 V 2.99 V	#2,98 V #2,98 V #3,02 V #3,04 V	
A5 #21,1NA 6A #21,1NA 6A	22,3NA 20.9NA 20.4NA 20.5NA	3.04 V 2.91 V 2.93 V 2.93 V	-3,08 V -2,94 V -2,91 V -2,93 V	
CS2 =22,3NA (22.0NA 22.8NA 21.4NA 21.8NA	2.98 V 3.03 V 2.96 V 2.97 V	-3,00 V -3,04 V -2,99 V -3.01 V	
DI1 =19,5NA DI2 =21,7NA	20.2NA 20.3NA 22.6NA 22.1NA	2.98 V 2.96 V 3.06 V 3.03 V	-2,94 V -2,93 V -3,00 V -2,98 V	

RÇA	CDP1822SD	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP:
					PAGF
	DOM	001	san	003	
00L1	115.MV 125.MV	120,MV 130.MV	130.MV 155.MV	130, MV 150. MV	
VOH1	4.82 V 9.74 V	4.82 V 9.75 V	4.82 V 9.74 V	4,82 v 9,75 v	
ION1	6,40MA 15,3MA	6.20MA 14.3MA	5.70MA	5'.80MA	
IDP1	=2.20MA =4.88MA	-2.21MA -4.91MA	12.6MA +2.15MA +4.71MA	13.0MA -2.19MA -4.92MA	
1021	134.NA	130 NA	141.NA	132,NA	
1072	133.NA 133.NA	131.NA 128.NA	134.NA 138.NA	138, NA 135, NA	
1024	131.NA 133.NA	133,NA 131,NA	131.NA 137.NA	140.NA	
10Z6 10Z7	122.NA 188.1	140.NA 131.NA	136.NA 145.NA	134,NA 131,NA	
1028	131.414	136.NA	133.NA	141.NA	
ILOP	=10,0UA				
IL:	=35,0UA =35,0UA				
IL3 IL4	≖35,0UA ≖25,0UA				

85 C

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SN:

PAGE	9 0	F 10
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		PAGE 9 UF
PASSED GALPAT (TIGHT	LIMITS) VCC=10V LIMITS) VCC=10V LIMITS) VCC=5V	REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR
PASSED DATA RETENTION	TEST	
	VCC = 4.5V	5'.0v 10'.0v
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA) 255.N (TDS) 24,0N (TDH) 14.0N	220'N 105.1 20.0N 8.707 14.0N 14.0N

ADDRESS ACCESS TIME	(TAA)	255.N	220.N	105.N
DATA SETUP TIME	(TDS)	24,0N	20.0N	8.70N
DATA HOLD TIME	(TDH)	14.0N		4.0 (2.1)
ONIN HORIT LINE	(IUN)	14 * 844	14.0N	14.0N
ADDRESS SETUP TIME	(TAS1)	4.00N	4.00N	A GGN
				4 . P Ø N
ADDRESS SETUP TIME	(TASE)	158°N	114.N	62.0N
ADDRESS HOLD TIME	(TAH)	-18,0N	=16.9N	-6.00N
WRITE PULSE WIDTH	(TWP)	48 0N	78.9N	44 0N
	• • • • • • • • • • • • • • • • • • • •	70 g Q . 1	1 G 8 -311	-4 -4 B \$112
CS1 SETUP TIME	(TCSS1)	184 N	162 N	94 78
CS2 SETUP TIME			10E 10	86,0N 84,0N
	(TCSS2)	182.N	158.N	84 ₀ (N
CS1 HOLD TIME	(YESH1)	54,0N	48.0N	30,0N
CS2 HOLD TIME	(TCSH2)	58.0N	50.0N	28'. ØN
	•	• •		
OUTPUT ACTIVE FROM CS1	(TDGA1)	258.N	550°N	114.N
OUTPUT ACTIVE FROM CS2	(TDDAZ)	254.N	224.N	
		,		114 N
OUTPUT ACTIVE FROM MRD	(TDOA3)	60.0N	54.0N	35.0N
# 1 TO 1 TO 1 TO 1 TO 1 TO 1 TO 1 TO 1 T				
OUTPUT HOLD FROM CS:	(TDOH1)	154,N	122,N	38, QN
OUTPUT HOLD FROM CS2	(SHOOT)	150 N	120,N	38 ្គឹ ២៧
OUTPUT HOLD FROM MRD	(TDOH3)	140.N	4 4 2 1	20 01
	•	***	118 N	38, QN
OUTPUT HOLD FROM MWR	(TPDH)	136,N	114 N	40.0N
READ CYCLE TIME	(TRC)	280.N	248,N	136.N
WRITE CYCLE TIME	(TWC)	248 N	224.N	136.M
		E 6 14	医左右单位	730 *

	IIL	IIH	AICI	A I C S
AØ	-125.NA	123 NA	2,93 V	
A1	#124.NA	125,NA	2,96 V	#2.97 V
A2	-127.NA	124.NA	2.98 V	#2,97 V #3,02 V
A3	-132.NA	123.NA	2.99 V	-3.04 V
A 4	-131.NA	128 NA	3.04 V	-3,08 V
A5	=121.NA	118 NA	2,90 V	-2,94 V
A6	-121 NA	115,NA	2.92 V	-2,91 V
A 7	=118.NA	115.NA	2.91 V	=2.93 V
CSi	≈133.NA	124.NA	2.97 V	=3,00 V =3,03 V
CSE	#130 NA	129,NA	3.01 V	-3.03 V
MWR	=130,NA	124 NA	2.96 V	#2,98 V
MRD	-130 NA	125'NA	2,97 V	-3.01 V
DIØ	#117.NA	117 NA	2,97 V	-2,93 V
DII	#115.NA	116.NA	5 96 A	#8,91 V
DIS	=124.NA	122, NA	3,06 V	-2,99 V
013	#120.NA	123.NA	3.03 V	-2.97 V

RCA	CDP:822SD	256 X 4	CMOS STATIC RAM	31 AUG 78	TEMP:	125 C	SN:	30
					PAGE	10 OF 5	10	

	מממ	100	200	003
VOL1	130.MV	135,MV	150.MV	145 MV
VOLS	140 MV	150.MV	170.MV	170 MV
VOH1	4.80 V	4 80 V	4.80 V	4 ู้ 80 V
VOHS	9.72 V	9.72 V	9.70 V	9.71 V
IONE	5.65MA	5.50MA	5.05MA	5,15MA
IDN2	13.6MA	12.6MA	11.2MA	11.4MA
IDP1	-1.97MA	-1.99MA	-1.93MA	-1,98MA
TOP2	-4.34MA	-4.41MA	-4.23MA	-4.39MA
1021	534.NA	578,NA	579.NA	564 NA
1072	531.NA	569,NA	584.NA	562,NA
1023	527,NA	569,NA	579.NA	561,NA
1024	532.NA	561.NA	583.NA	564.NA
1025	531.NA	571,NA	593.NA	573, NA
1026	542.NA	569,NA	579.NA	577,NA
1077	528.NA	576.NA	579.NA	569,NA
1028	535.NA	562.NA	587.NA	567.NA
ILDP	20,0UA			
ILi	-85.0HA			
ILZ	-100.UA			
11.3	-85,0UA			
IL4	-70.0UA			
	- ··			

PAGE 1 OF 10

PASSED	GALPAT	(WIDE	LIMITS)	VCC=10V	REPRODUCIBILITY OF THE
			LIMITS) LIMITS)	100-407	ORIGINAL PAGE IS FOOR
	AWM. WI	Č. Prittir	W4114142	1120-21	OTTO - IN-

PASSED DATA RETENTION TEST

	,			
	VCC	= 4.5V	5.0V	10'.0V
ADDRESS ACCESS TIME	(TAA)	265.N	270,N	95.0N
DATA SETUP TIME	(TDS)	24,ØN	20,QN	8.00N
DATA HOLD TIME	(TDH)	12.ØN	10,QN	12.0N
ADDRESS SETUP TIME	(TAS1)	18,0N	14.0N	4 . 00 N
ADDRESS SETUP TIME	(TAS2)	124.N	106.N	54 . 0 N
ADDRESS HOLD TIME	(TAH)	-18,0N	=16.0N	-6 . 00 N
WRITE PULSE WIDTH	(TWP)	76.0N	64.0N	38 . 0 N
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS1)	180 m	154°N	78,0H
	(TCSS2)	174 m	150°N	76,0H
	(TCSH1)	38 on	34°ON	22,0H
	(TCSH2)	40 on	34°ON	22,0H
OUTPUT ACTIVE FROM CS	(SAOGT) Si	248.N	214.N	102.N
OUTPUT ACTIVE FROM CS		246.N	212.N	98.0N
OUTPUT ACTIVE FROM MR		56.0N	50.0N	28.0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH!) (TDOH2) (TDOH3) (TPOH) (TRC) (TWC)	150 m 146 m 138 m 134 m 272 m 256 m	118, N 116, N 116, N 112, N 232, N 192, N	32,0N 32,0N 36,0N 38.0N 128.N
IIL	IIH	VICI	VICP	
A0 91.70NA	1,30NA	3.00 V	-2,98 V	
A1 #1.40NA	1,20NA	3.02 V	-3,04 V	
A2 #1.70NA	1,50NA	3.03 V	-3,09 V	
A3 #1.30NA	1,30NA	3.05 V	-3,05 V	
A4 #1.30NA A5 #1.40NA A6 #1.60NA A7 #1.90NA	1,30NA 1.30NA -1,60NA 1.40NA	3.05 V 3.03 V 2.99 V 3.01 V	#3.04 V #3.05 V #3.06 V	
CS1 =1.40NA	1,20NA	3.05 V	35,02 V	
CS2 =1.40NA	1,50NA	3.08 V	-3,07 V	
MWR =2.00NA	1,30NA	3.01 V	-3,01 V	
MRD =1.60NA	1,40NA	2.98 V	-3,02 V	
DIO #1.60NA	1,20NA	3.13 V	=3 07 V	
DI1 #2.60NA	1,20NA	3.13 V	=3 06 V	
DI2 #1.40NA	1,30NA	3.13 V	=3 04 V	
DI3 #1.30NA	1,30NA	3.13 V	=3 07 V	

RCA	CDP1822SD	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP:	as c s	N :
					PAGE	2 OF 10	
	ממס	1001	500	003			
VULI	110.MV	115,MV	125.MV	125, HV			
AOLS	115.MV	125.MV	140 MV	140 MV			
VOH1	4.84 V	4,83 V	4.83 V	140 MV 4 84 V			
AOHS	9.76 V	9,76 V	9.76 V	9.76 V			
ION1	6.65MA	6.40MA	6.Ø5MA	6 05MA			
1045	16.3MA	15.1MA	13.6MA	13.8MA			
IDPi	-2.35MA	- r	#2.31MA	#2,33MA			
1092	⇔5.23MA	-5.22MA	#5.06MA	~5.24MA			
IOZI	28,0NA	24.8NA	29.7NA	23.4NA			
1025	24.1NA	27.9NA	56, SNV	26.8NA			
1073	29.7NA	23,1NA	30,5NA	23,4NA			
IUZ4	29,5NA	22.1NA	31.6NA	21.6NA			
1025	24,1NA	29,1NA	25, 2NA	29.3NA			
1026	23,7NA	28.6NA	25,3NA	29.2NA			
IUZ7	24,5NA	29.1NA	25, 1NA	ANR.8S			
1028	23.9NA	AN8,85	25"2NA	28.6NA			
ILDP	≈15,011A						
IL1 IL2 IL3 IL4	⇔30.0UA ⇔25.0UA ⇔30,0UA ⇔25.0UA						

RCA	CDP1822SD	256 X 4	CMOS STA	TIC RAM	31	AUG 78	TEMPI	#20 C	SNI	31
-							PAGE	3 OF	10	

PASSED	GALPAT	CWIDE	LIMITS	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS)	VCC=10Y
PASSED	GALPAT	(TIGHT	LIMITS)	VCC=5V

PASSED DATA RETENTION TEST

	vcc	= 4.5V	5.øv	1.0 ° av
ADDRESS ACCESS TIME	(TAA)	10.8N	215'N	55.0N
DATA SETUP TIME	(TDS)	26.8N	22.0N	8.00N
DATA HOLD TIME	(TDH)	16.8N	10.0N	10.0N
ADDRESS SETUP TIME ADDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WIDTH	(TAS1) (TAS2) (TAH) (TWP)	18.0N 120.N -18.0N 78.0N	94 ª dN ≈14 ª dN €14 ª dN	4 m 00 N 4 B m 00 N = 4 m 00 N 3 G m 00 N
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS1)	170.N	146' N	70,0N
	(TCSS2)	166.N	142' N	70,0N
	(TCSH1)	36.0N	32' N	22,0N
	(TCSH2)	38.0N	34' N	20,0N
OUTPUT ACTIVE FROM CS	(SADOT) SE	244.N	202' _F N	94,0N
OUTPUT ACTIVE FROM CS		240.N	200' N	90,0N
OUTPUT ACTIVE FROM MR		52.0N	46' NN	26.0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDGH1) (TDGH2) (TDGH3) (TPDH) (TRC) (TWC)	142.N 140.N 134.N 132.N 256.N 248.N	110 N 108 N 114 N 110 N 216 N 248 N	28,0N 28,0N 32,0N 34.0N 120.N
IIL	IIH	VIC1	vica	
A0 +400.PA	200.PA	3.07 V	-3,04 V	
A1 +200.PA	200.PA	3.09 V	-3,11 V	
A2 +300.PA	200.PA	3.09 V	-3,14 V	
A3 +200.PA	200.PA	3.11 V	-3,11 V	
A4 =300.PA	200,PA	3.11 V	#3,13 V	
A5 =200.PA	200,PA	3.09 V	#3,13 V	
A6 =300.PA	300,PA	3.05 V	#3,13 V	
A7 =400.PA	200,PA	3.08 V	#3,11 V	
CS1 =200.PA	200,PA	3.12 V	+3,09 V	
CS2 =200.PA	300,PA	3.14 V	+3,13 V	
MWR =300.PA	200,PA	3.08 V	+3,07 V	
MRD =400.PA	500.PA	3.05 V	+3,09 V	
DIO =300.PA	200,PA	3.19 V	#3,13 V	
DI1 =600.PA	200,PA	3.18 V	#3,12 V	
DI2 =200.PA	200,PA	3.19 V	#3,11 V	
DI3 =200.PA	200.PA	3.18 V	#3,13 V	

RCA	CDP1822SD	256	X	4	CMOS	STATIC	RAM	31	AÚG	78	TEMP:	- 20	¢	SN#	31
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μ	Δ	GE	- 4	OF	110

	naa	001	005	D03
VOL 1	100.MV	105,MV	110.MV	110,MV
Aors .	100.MV	110 MV	120.MV	i a a . Mv
VOH1	4,86 V	4.86 V	4.86 V	
VOHE	9.80 V	9.80 V	9.80 V	4,86 V 9,80 V
V 01.1C	v # cata A	7 . UD V	7 u U u V	A WILLIAM
ION1	7.50MA	7.15MA	6.85MA	6.80MA
IDNS	18.7MA	17.3MA	15.7MA	15,9MA
IDPI	-2.79MA	-2,81MA	#2.77MA	H2,78MA
IDP2	-6.21MA	₩6,29MA	=6.11MA	AMES. 6*
10. 5	- ri fit file	WO ALL YOR	#OF FINA	word dama
1071	2.50NA	6.80NA	1.40NA	6,80NA
10Z2	5,20NA	3.50NA	3,70NA	4 101114
IOZ3	4.00NA	3,30NA	4.80NA	4,10NA 2,40NA
1024	1.20114	6,90NA	1_80NA	5 80NA
* :: " ·	CBMONIA	A W AND CO	# # CAKIMAN	21 2 C) 1/1 (4 M)
1025	7.20NA	1.40KA	6.50NA	S, GONA
1076	7.50NA	1.40NA	6.10NA	2.10NA
7077	6.90NA	1,5UNA	6.30NA	2,19NA 2,19NA
IOZ8	7.30NA	1,60NA	6.00NA	2.INNA
***	1 Back and	4 5 5 5 7 7	O a world be	C B Tailet
ILDP	- 5.00U∧			
N 14:11	- 2 B W M D W			
ILI	-25,0UA			
ILS	-20.0UA			
IL3	-25.0UA			
114	#50.0UA			
4 14 44	ったい。ないハ			

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RCA CDP1822SD 256 X	4 CMOS STATIC RAM	31 AUG 78 TEMPI	-55 C SN: 3
		PÄGE	5 OF 10
PASSED GALPAT (WIDE PASSED GALPAT (TIGHT PASSED GALPAT)	LIMITS) VCC=10V	REPRODUCIBILIT ORIGINAL PAGE	y of the is foor
PASSED DATA RETENTION	TEST		
	VCC = 4,5V	5.øv	10.0V
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA) 255.N (TDS) 32.0N (TDH) 8.00N	205 <u>"</u> n 24"qn	80 0N 8 00N 10 0N
ADDRESS SETUP TIME ADDRESS SETUP TIME AUDRESS HOLD TIME WRITE PULSE WIDTH	(TAS1) 16.0N (TAS2) 118.N (TAH) -18.0N (TWP) 82.0N	12,0N 96,0N -14,0N 60,0N	4.00N 42.0N -4.00N 36.0N

66,0N 64,0N 22,0N 20.0N

88,0N 86,0N 24.0N

24,0N 24,0N 30,0N 32,0N 120,N

CASE SECTION

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DATA MI	ILD TIME	(TDH)	8 . @ØN	8 * 00N	
ADDRESS AUDRESS	S SETUP TIME S SETUP TIME S HOLD TIME PULSE WIDTH	(TAS1) (TAS2) (TAH) (TWP)	16.0N 118.N -18.0N 82.0N	12,0N 96,0N -14,0N 60,0N	
CS2 SE		(TCSS1) (TCSS2) (TCSH1) (TCSH2)	166 N 162 N 42 ON 44 ON	136, N 138, N 34, ON 38, ON	
OUTPUT	ACTIVE FROM CS ACTIVE FROM CS ACTIVE FROM ME	SE (TDOAE)	246.N 242.N 48.ØN	198, N 196, N 42. ON	
OUTPUT OUTPUT CUTPUT READ C	HOLD FROM CS1 HOLD FROM MRD HOLD FROM MUR YCLE TIME CYCLE TIME	(TDOH1) (TDOH2) (TDOH3) (TPOH) (TRC) (TWC)	136.N 132.N 132.N 132.N 232.N 240.N	102, N 100, N 112, N 108, N 200, N 272, N	
	IIL	IIH	VICI	vica	
	FIL *100.PA #100.PA *100.PA 0.00 A	IIH 100'.PA 0.00 A 100,PA 100.PA	VIC: 3.14 V 5,17 V 3.16 V 3.18 V	#3,13 V #3,18 V #3,21 V #3,18 V	
A 1 A 2 A 3	9100.PA 9100.PA 9100.PA	100.PA 0.00 A 100,PA	3.14 V 3,17 V 3.16 V	#3,13 V #3,18 V	
A1 A2 A3 A4 A5 A6	*100.PA *100.PA *100.PA 0.00 A *100.PA 0.00 A *100.PA	100.PA 0.00 A 100.PA 100.PA 100.PA 100.PA 100.PA	3.14 V 5,17 V 3.16 V 3.18 V 3.18 V 3.16 V 3.15 V	#3,13 V #3,18 V #3,21 V #3,18 V	
A1 A2 A3 A4 A5 A6 A7 CS2 MWRD DI1 DI2	*100.PA *100.PA *100.PA *100.PA *100.PA *100.PA *100.PA *100.PA *100.PA *100.PA *100.PA *100.PA	100.PA 100.PA 100.PA 100.PA 100.PA 100.PA 100.PA 100.PA 100.PA 100.PA	3.14 V 3.17 V 3.16 V 3.18 V 3.18 V 3.15 V 3.20 V 3.21 V	73713 V 73718 V 73718 V 73718 V 73718 V 73718 V 73718 V 73718 V 73718 V	

RÇA	CDP18225D	256 X	4	CMOS	STATIC	RAM	31	AUG	78	TEMP:	# 55	Ç	SN:	31
										PAGE	6	OF	10	

	ùOα	001	200	203
VOL 1	90.0HV	95.ØMV	100.MY	190, MV
VUL2	90.0MV	100 MV	110 MV	เตรูโหง
VOH1	4.88 y	4,88 V	4.88 V	4,88 V
SHOV	9 83 V	9.83 V	9.83 V	9 84 V
ION1	8.15MA	7.80MA	7.45MA	7.40MA
IONS	20.7MA	19.2MA	17.5MA	17.7MA
IOP1	⇔3.18MA	-3,25MA	-3.21MA	±3,21MA
1055	-7.10MA	-7.19MA	-7.03MA	-7.18M4
1021	4 . 80NA	400.PA	2.70NA	,1,30NA
1025	5.70NA	-1,7MNA	5.40NA	-1,30NA
1023	-1.30MA	5,30NA	-1.50NA	5,50NA
1024	400 PA	3.40NA	-800.PA	4 40NA
1075	4.20NA	-1,10NA	4.60NA	-1,50NA
1026	4 40 MA	-1,30NA	4.50NA	-1.50NA
IUZ7	4.30NA	-1.20NA	4.70NA	60NA م1•
1028	4.50NA	-1.40NA	4.70NA	-1.50NA
ILDP	-10.0UA			
ILI	~20.0UA			
ILS	-20,0UA			
IL3	₩20.0UA			
IL4	-15.0UA			

RCA COPIBEESD 256	X 4 CMOS STA	TIC RAM 3	1 AUG 78 TEMPÍ	85 C SN:
			PAGE	7 OF 10
PASSED GALPAT (TIGHT	T LIMITS) VC	C=10V C=10V C=5V		
PASSED DATA RETENTION	N TEST			
	vcc	≈ 4,5V	5'.ØV	10.0V
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA) (TDS) (TDH)	265.N 26.ØN 14.ØN	225 ¹ N 22.0N 12.0N	105.N 8.70N 12.0N
ADDRESS SETUP TIME ADDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WIDTH	(TAS1) (TAS2) (TAH) (TWP)	10.0N 137.N 10.0S 10.0N	8.00N 114.N -18.0N 76.0N	4.00N 60.0N -6.00N 44.0N
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS1) (TCSS2) (TCSH1) (TCSH2)	188 N 184 N 50 M 54 M	162 N 158 N 46 N 48 N	86,0N 84,0N 30,0N 28.0N
OUTPUT ACTIVE FROM CS OUTPUT ACTIVE FROM CS OUTPUT ACTIVE FROM ME	(SADOT) SE	256.N 254.N 60.0N	226, N 222, N 54, ØN	114.N 112.N 32.0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH1) (TDOH2) (TDOH3) (TPOH) (TRC) (TWC)	156.N 154.N 138.N 136.N 280.N	124, N 122, N 118, N 114, N 248, N 224, N	38,0N 38,0N 38,0N 40,0N 136,N
TIL	IIH	VIC1	AICS	
A0 =19.3NA A1 =19.0NA A2 =18.9NA A3 =18.5NA	18.5NA 18,2NA 19,3NA 18,3NA	2.97 V 2.99 V 3.00 V 3.02 V	-2,94 V -3,00 V -3,05 V -3,02 V	
A4 =17.9NA A5 =19.2NA A6 =19.1NA A7 =20.2NA	18.1NA 18.5NA 18,7NA 18,5NA	3.02 V 3.00 V 2.96 V 2.98 V	53,05 V -3,02 V -3,03 V -3,01 V	
CS1 =18,6NA CS2 =17,9NA MWR =18,5NA MRD =18,9NA	17.6NA 19.9NA 17.9NA 18.5NA	3.02 V 3.05 V 2.98 V 2.95 V	#2,99 V #2,98 V #2,98 V	
DIO =18,6NA DI1 =20,5NA DI2 =17,1NA DI3 =17,3NA	18.0NA 18.1NA 17.6NA 17.6NA	3,11 V 3,10 V 3,10 V 3,10 V	-3,04 V -3,03 V -3,01 V -3,04 V	

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RCA	CDP1822SD	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP:	85 C SN:	31
					PAGE	8 OF 10	
	DOM	001	soo	DOZ			
VOL1 VOL2 VOH1	130.MV 140.MV 4.80 V 9.72 V	135.MV 150.MV 4.80 V 9.72 V	145,MV 165,MV 4,80 V 9,71 V	145 MV 165 MV 4 80 V 9 72 V			
ION1 ION2 IOP1 IOP2	-1.97MA	5.50MA 12.7MA -1.99MA -4.45MA	5.20MA 11.5MA -1.95MA -4.31MA	5.20MA 11.7MA -1.96MA -4.42MA			
1021 1022 1023 1024	281.NA 278.NA 275.NA 278.NA	290,NA 284.NA 285.NA 279.NA	291 NA 295 NA 294 NA 300 NA	279'NA 272'NA 276'NA 273'NA			
1025 1076 1077 1028	279,NA 291,NA 280,NA 283,NA	287,NA 281,NA 292.NA 279.NA	304.NA 300.NA 295.NA 307.NA	281,NA 285,NA 283,NA 277.NA			
TLDP	1.8041						

-45.0UA -40.0UA -45.0UA -40.0UA

IL1 IL2 IL3 IL4

RCA CDP1822SD 256 X	4 CHOS STATEC RAM	31 AUG 78 TEMPE	125 C SN: 31
		PÁGE	9 OF 18
	LIMITS) VCC=10V LIMITS) VCC=10V LIMITS) VCC=5V	REPRODUCIBILITY ORIGINAL PAGE I	
PASSED DATA RETENTION	TEST	,	
	VCC = 4.5V	5 . 0v	10.pv
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA) 270 N (TDS) 26,0Ñ (TDH) 16.0N	235,N 22, ØN 16, ØN	115.N 10.0N 14.0N

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	VUL	, ≈ 4.⊐V	3.04	Th*bA
IBBOTOS IMBOS MULT				
ADDRESS ACCESS TIME	(TAA)	27Ø.N	235, N	115.N
DATA SETUP TIME	(YDS)	26,0N	22. ØN	10,0N
DATA HOLD TIME	(HOH)	16.0N	16.0N	14.2N
	E + MILLS	10891	102011	Tation
ADDRESS SETUP TIME	(TASL)	A MININ	6.00N	n naki
		6 . ØØN	D W CONTR	4 . PON
ADDRESS SETUP TIME	(TAS2)	140 N	124.N	68, ØN
ADDRESS HOLD TIME	(TAH)	=20°0N	-18.0N	NB 0 0 8 ₩
WRITE PULSE WINTH	(TWP)	94. ØN	84.0N	48. ØN
men , Omer Manin	r i n i J	24 * Fig.	O et # Kila	40 4 20
CS1 SETUP TIME	18000011	400 N	a man t	94 ØN 90 ØN
	(TCSS1)	198.N	174 N	94,00
CS2 SETUP TIME	(TCSS2)	194 N	170'aN	90 MN
CS1 HOLD TIME	(TCSH1)	56, ØN	50,0N	30,00
CS2 HOLD TIME	(TCSH2)	58, ØN		70 00
age units itue	Cicousi	NA GC	52.ØN	30.0N
AllThur Lording Show and	49604ib	**** ***	mm a f	
OUTPUT ACTIVE FROM CS1	(TDOAL)	270.N	238, N	126.N
OUTPUT ACTIVE FROM CS2	(SADOT)	266.N	234.N	128 N
OUTPUT ACTIVE FROM MRD	(TDOA3)	66.0N	58.0N	34.0N
	¥ 1 0 ~ 1	00.90.0	20 # 614	275111
OUTPUT HOLD FROM CS1	(TDOH1)	158 N	e Def N	42,0N
			128,N	45,400
OUTPUT HOLD FROM Cap	(SHOOT)	1,56 . N	156 V	42,0N
OUTPUT HOLD FROM MRD	(TOOH3)	138.N	118 N	40,0N
OUTPUT HOLD FROM MWR	CHOSTS	140.N	116.N	40.0N
READ CYCLE TIME			1000	
	(TRC)	296 N	256 N	152.N
WRITE CYCLE TIME	(TWC)	264.N	240°N	144.N
IIL II	H	VICI	AICS	
AØ =110,NA 10	7 NA	2.97 V	=2,94 V	
A1 -110.NA 10	D NA			
	8 NA	2,99 V	-3,00 V	
A2 #107.NA 10	BPNA	2,99 V 3,00 V	-3,00 V -3,06 V	
A3 9106.NA 10	4.NA	3.02 V	•3.02 V	
-				
A4 ~105.NA 10	4 NA	3,02 V	,3,06 V	
			Sandario A	
	7 - NA	3.00 V	43 NG A	
A6 #109.NA 10	4°NA	2.95 V	ლ3,03 V	
A7 #112.NA 10	5.NA	2.98 V	+3,03 V +3,03 V +3,00 V	
	-			
CS1 #109,NA 10	۸۸ م 2	3,02 V	#2,99 V #3,05 V #2,97 V	•
CS2 -104 NA 10	Q NA	지 (BE 1) 기술되다 1	# # # # # # # # # # # # # # # # # # #	
	BPNA	3,05 V	•3,05 V	
MWR =104.NA 10	1 NA	2,98 V	#2,97 V	
	4.NA	2.95 V	-2.99 V	
	_			
DIO -106.NA 10	5 NA	3,11 V	-3,04 V	
DI1 -108.NA 10	3.NA	3,10 V	-3,02 V	
		~ 5 ¥ € € €	THE V	
	. SNA	3,10 V	-3,02 V -3,01 V	
DI3 =99,9NA 10	1 . NA	3.10 V 3.10 V	#03.04 V	
		• •	· · · · · ·	

RÇA	CDP182250	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP	125 C SN:
					PAGF	10 OF 10
	ממח	001	Doa	003		
VOL 1	145 MV	150 MV	160.MV	160.MV		
vor5	155,MV	170.MV	190 MV	1,85 MV		
VOH1	4.78 V	4,78 V	4,77 V	4,78 V		
AOHS	9.68 V	9.68 V	9,67 V	9_68 V		
I I N I	5,15MA	4.90MA	4,65MA	4.70MA		
IDNS	12.3MA	11.3MA	10.2MA	1 M . AMA		
IDP1	-1.78MA	-1.78MA	#1,75MA	=1,78MA		
IOP2	₩3.97MA	-3,95MA	-3"A8MA	#3.99MA		e e e e e e e e e e e e e e e e e e e
1021	AUE5.1	1.2304	1,27UA	1,2104		
IOZ2	1.21HA	1,23UA	1.26UA	1,2204		
1023	1.22114	1.22UA	1.27UA	1,2104		
1074	1,21UA	1.22UA	1.26UA	1.2204		
IUZS	1.2304	1,2404	1.30UA	2504م 1		
1076	1.24UA	1,2404	1.2904	1,2204		
1027	1.23UA	1,2404	1.28UA	1,2204		
1078	1.5507	1.2404	1.27UA	1.23UA		

ILDP	40°00A
IL.	-105,UA
ILS	-110.UA
IL3	-110 UA
71 A	-90 BUA

RCA CDP1822SD 256 X	4 CMOS STA	TIC RAM 31	AÚG 78 TEMPÍ	as c sni
•			PAGE	1 OF 10
PASSED GALPAT (WIDE PASSED GALPAT (TIGHT PASSED GALPAT (TIGHT	r Limita) vçi	C=10V C=10V C=5V		
FAILED DATA RETENTION	TEST ADD #	16 DÍAG #	Ø PIN: ØĨ7	
	VCC	= 4.5V	5 . ØV	10.0V
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA) (TDS) (TDH)	265°N 18' QN 13' QN	215'N 16,0N 12.0N	85,0N 8,00N 12,0N
ADDRESS SETUP TIME ADDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WIDTH	(TAS1) (TAS2) (TAH) (TWP)	8.00N 128.N -18.0N 64.0N	8.00N 100.N *14.0N 56.0N	4 - 00N 44 - 0N - 4 - 00N - 3 - 0N
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TC851) (TC882) (TC8H1) (TC8H2)	0 . 00 0 . 00 0 . 00	6,00 6,00 6,00 6,00	60,0N 56,0N 14,0N 14.0N
OUTPUT ACTIVE FROM CS OUTPUT ACTIVE FROM ME OUTPUT ACTIVE FROM ME	(SAOOT) SE	0.00 0.00 52.0N	0,00 0.00 46.0N	96°0N 90°0N 95°0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH1) (TDOH2) (TDOH3) (TPOH) (TRC) (TWC)	300. N 300. N 138. N 136. N 280. N 192. N	300, N 300, N 110, N 110, N 124, N 176, N	18,0N 20,0N 32,0N 32,0N 120,N
IIL	IIH	VICI	AICS	
A0 =12.0NA A1 =16.6NA A2 =8.20NA A3 =6.40NA	3,60NA 3,70NA 2,80NA 2,70NA	3.10 V 3,15 V 3,15 V 3.16 V	-3,10 V -3,14 V -3,17 V -3,15 V	
AG .E. EA ANGL.E. EA AG .E. AA ANGL.E. TA	2'.70NA 3.40NA 3.40NA 2.90NA	3.18 V 3,09 V 3,11 V 3,12 V	-3,18 V -3,15 V -3,14 V -3,14 V	
CS1 =3.20NA CS2 =3,00NA MWR =5,40NA MRD =3,40NA	4,00NA 3,30NA 2,90NA 2.80NA	3,15 V 3,17 V 3,11 V 3,14 V	#3,15 V #3,17 V #3,11 V #3,13 V	
DIO =2.60NA DI1 =2.50NA DI2 =2.80NA DI3 =3.20NA	2,90NA 2,90NA 3,20NA 3,00NA	3.23 V 3.20 V 3.22 V 3.22 V	-3,19 V -3,17 V -3,19 V -3,16 V	

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RÇA	CDP1822SD	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP:	25 C SN;
					PAGE	2 OF 10
	DOD	001	Soo	003		
VOL 1	105.MV 110.MV	110'.MV 120.MV	120,MV 130,MV	115 MV		
VOH	4,86 V	4,85 V	4.85 V	130 MV 4.86 V		
V0H5	9,78 V	9.78 V	9.78 Y	9,79 V		
IDNI	6.80MA	6.50MA	6.15MA	6,25MA		
IDNE	17,4MA	15.9HA	14,5MA	14.7MA		
TOP 1	M00.5m	-2,64MA	≈2,59MA	+2,67MA		
IDP2	-5.81MA	₩5.81MA	#5.62MA	=5,91MA		
TOZI	10,2UA	10.2UA	tø¦sn∀	10,244		
IOZS	12,3NA	9.70NA	9.50NA	ANS.DI		
1023	AUS, DI	10.2UA	10.2UA	id.5NA		
TUZ4	10.0NA	12.3NA	7.10NA	12,4NA		
1025	-10,2UA	-10.2UA	-10,2UA	-im_auA		
1026	13,2NA	9,90NA 9,10NA	12,2NA	7,80NA		
1027	13,3NA	9,10NA	12,4NA	7,60NA		
1028	13,5NA	8 390NA	12,4NA	7 . 1 @NA		
ILDP	190.UA					
ILi	-10.0UA					
ILS	-10.0UA					
IL3	-10,0UA					
IL4	#15,0UA					

PAGE 3 OF 10

PASSED GALPAT (WIDE PASSED GALPAT (TIGHT PASSED GALPAT (TIGHT	T LIMITS) VC	C=10V C=10V C=5V	REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR
FAILED DATA RETENTION	TEST ADD *	16 DIAG #	Ø PIN: Ø17
	VCC	= 4 _m 5V	5'. 0V 10'. 0V
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA) (TDS) (TDH)	285°N 50°0N 10°0N	210'N 75'.0N 16.0N 6.00N 10.0N 10.0N
ADDRESS SETUP TIME ADDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WINTH	(TAS1) (TAS2) (TAH) (TWP)	12.0N 126.2N -18.0N -66.0N	10.0N 4.00N .100.N 40.0N =14.0N -2.00N 58.0N 30.0N
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS1) (TCSS2) (TCSH1) (TCSH2)	ମ • ମପ ମ • ମଧ ମ • ମଧ ମ • ଅଧ	0.00 54.00 0.00 52.00 0.00 10.00 0.00 10.00
OUTPUT ACTIVE FROM CS OUTPUT ACTIVE FROM CS OUTPUT ACTIVE FROM ME	S2 (TDOA2)	0.00 0.00 50.0N	0,00 74,0N 0.00 72,0N 42.0N 24.0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH1) (TDOH2) (TDOH3) (TPOH) (TRC) (TWC)	300 N 300 N 134 N 134 N 256 N 192 N	300 N 14.0N 300 N 14.0N 112 N 30.0N 163 N 30.0N 208 N 112 N
TIL	IIH	VICI	VTC2
A0 =500.PA A1 =800.PA A2 =500.PA A3 =500.PA	300.PA 400.PA 300.PA 300.PA	3.82 V	-3,18 V -3,22 V -3,24 V -3,23 V
A4	400,PA 400,PA 400,PA 300.PA	3.25 V 3.16 V 3.18 V 3.19 V	#3,26 V #3,28 V #3,28 V
CS1 =400.PA CS2 =300.PA MWR =800.PA MRD =400.PA	500,PA 300,PA 400,PA 300,PA	3.24 V 3.18 V	-3,23 V -3,24 V -3,18 V -3,21 V
DIO -300.PA DII -300.PA DI2 -300.PA DI3 -400.PA	300 PA 300 PA 400 PA 400 PA	3,30 V 3,28 V 3,29 V 3,29 V	-3,26 V -3,26 V -3,26 V

B-313

RCA	CDP1822SD	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP:
					PAGF
	מסמ	001	500	png	
VOLI	95,0MV	100,MV	105.MV	105, MV	
AULS	95.0MV	100.MV	115.MV	110.MV	
VOH1	/Las v	4,88 V	4.88 V	4 88 V	
A0H5	9.82 V	9.82 V	9.82 V	9 83 V	
IDN	7.60MA	7 25MA	6.95MA	7 <u>'</u> 09MA	
IUNS	19.9MA	18.3MA	16.5MA	17.0MA	
IDP1	-3,11MA	-3,13MA	#3.ØBMA	e3,13MA	
IDP2	=6.84MA	⇔6.88MA	⇔6.67MA	-6.95MA	
1021	11.5NA	3.10NA	9,40NA	3.5004	
1025	7.3ENA	500.PA	6.80NA	-100.PA	
1023	12.2NA	18.3NA	15.1NA	21.6NA	
1024	5.10NA	3.00NA	3.40NA	3, GWN A	
1025	-10,2114	-10.20A	-10'_2UA	-10.2UA	
1076	1.4004	6,90NA	700.PA	6 4 M N A	
1027	1.50NA	7.20NA	600.PA	6,30NA	
1028	1.50NA	7.00NA	800.PA	6.30NA	
ILDP	155 _# UA				
IL1	-5.00UA				
TLP	~5.00UA				
IL3	-10.0UA				
IL4	-10.0UA				

#20 C

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SNI

PASSED GALPAT (WIDE LIMITS) VCC=10V PASSED GALPAT (TIGHT LIMITS) VCC=10V PASSED GALPAT (TIGHT LIMITS) VCC=5V

FAILED DATA RETENTION	N TEST ADD =	16 DTAG	m 0 PIN:	ต 1 7
	VCC	= 4.5V	5.0V	10'.0V
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA) (TDS) (TDH)	285.N 24.gn 8.gan	200. 18. MN 8. MM	70.0N 6.00N 10.0N
ADDRESS SETUP TIME ADDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WIDTH	(TAS1) (TAS2) (TAH) (TWP)	12.0N 130.N -18.0N 70.0N	8,00N 98,0N =12,0N 54,0N	4.00k 36.0k 4.00k
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS1) (TCSS2) (TCSH1) (TCSH2)	0 • 00 0 • 00 0 • 00 0 • 00	ଉ' ₋ ଥେଉ ଉ ₋ ଥେଉ ଉ ₋ ଥେଉ	52,0N 48,0N 12,0N 12.0N
OUTPUT ACTIVE FROM CS OUTPUT ACTIVE FROM CS OUTPUT ACTIVE FROM ME	(SADOT) SE	0	0.0A 0.0A 3A.0N	70,0N 66,0N 22.0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH1) (TDOH2) (TDOH3) (TPOH) (TRC) (TWC)	300.N 300.N 134.N 132.N 232.N	300, N 300, N 110, N 106, N 200, N 176, N	12.0N 12.0N 28.0N 28.0N 104.N
IIL	IIH	VICI	VICE	
A0 -100.PA A1 +100.PA A2 +100.PA A3 +100.PA	100.PA 100.PA 100.PA 100.PA	3.24 V 3.29 V 3.29 V 3.30 V	#3,25 V #3,29 V #3,31 V #3,29 V	
A4 =100.PA A5 =100.PA A6 =100.PA A7 =100.PA	100.PA 100.PA 100.PA 100.PA	3.32 V 3.25 V 3.26 V	-3,32 V -3,29 V -3,29 V	
CS1 = 100,PA CS2 = 100,PA MWR = 200,PA MRD = 100,PA	100.PA 100.PA 100.PA 100.PA	3.29 V 3.31 V 3.25 V 3.29 V	73/29 V 73/30 V 73/24 V 73/28 V	
DIO -100.PA DI1 =100.PA DI2 =100.PA DI3 =100.PA	100 PA 100 PA 100 PA 100 PA	3.37 V 3.35 V 3.36 V 3.36 V	T3,33 V T3,31 V T3,35 V T3,29 V	

RCA	CDP18228D	256	X 4	CMOS	STAT	IC	RAM	31	AUG	78	TEMP:	~55	C	SN:	
											PAGE	6	OF	10	
	noø		001			נסמ	9		Di	73					
VOL.1	90.0MV		95.	ØMV		95	ØMV		9:	5.MNV					
VOLZ	85.ØMV		90.	ØMV		10	S.MV		1.9	VM. NO					
VOH1	4.89 V		4 . 8	9 V		4 . 8	39 V		4	89 V					
VUHE	9.84 V			5 V			34 V		9	5.0MV 70.MV .89 V .85 V					
IDN1	8.30MA			SMA		7.	БОМА			65MA					
SNOT	AM0.59			4MA			6MA		1 9	A MP .					
IUPi	≃3.61MA		-3,6	AMS:	647	3.	57MA			65MA					
1092	-7 -97MA		-8.€	IMA	**	7 .	75MA		=8	.11MA					
1021	4.50NA		-100			-	10NA		-8	gg.PA					
IUZZ	600.PA		3 . 5	MNA		40	Ø.PA		5	SONA					
IDZ3	4.PGNA		300	I.PA		2.	90NA		. 1	"50MY					
IOZ4	6.MGNA		-1.7	NA		5.	ANDR		 1	- GUNA					
1075	-10.2UA		-10.	AUS.			. BUA			M.PUA					
1026	5.50NA		1,7	ØNA		1.	OONA		2	711NA					
1027	2,60NA		و ۾ ا	AMDI		80	M.PA		5	, 60NA					
1028	2.40NA		1.7	' (PNA		1.	1 ØN A		5	. 70NA					
ILDP	160.HA														
ILi	~5_0UUA														
īĽŝ	≈5.00HA														
IL3	-5.00UA														
IL 4	=5.00UA														

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PASSED GALPA PASSED GALPA PASSED GALPA	T (TIGHT LI	MITS) VC	C = 1 0 V C = 1 0 V C = 5 V	REPRODUCIBILITY ORIGINAL PAGE	OF THE IS POOR
FAILFD DATA	RETENTION TE	ST ADD =	16 DIAG	# 0 PTN: 01	7
		Vac	# 4.5V	5 . øv	10.0v
ADDRESS ACCE	SS TIME	(TAA)	250.N	210 <u>'</u> N	90.00
DATA SETUP T		(TDS)	18, ØN	16.NN	8. 7. ØN
DATA HOLD TI	ME	(нат)	14.0N	14.0N	14.0N
ADDRESS SETU		(TAS1)	6.00N	6 nmn	4.90N
ADDRESS SETU		(TASE)	150.0	100.N	50.0N
ADDRESS HOLD		(TAH)	-16,0N	₩14.ØN	-4.00N
WRITE PULSE	MIDIH	(TWP)	70.0N	62. an	38.0N
-	TIME	(TCSS1)	ପ୍ରପ୍ର	ผ _ู ้ ผล	62, ØN
	TIME	(TCSS2)	7.00	ପ୍ରକୃତ୍ତ	62,0N
CS1 HOLD T		(TCSH1)	п.ор	0,00	14,ØN
CSS KOLD T	IME	(TCSH2)	a • aa	ด้. ผส	14.0N
OUTPUT ACTIV	E FROM CS1	(TDOA1)	ପ୍ରପ୍ର	ด์ ผล	90,0N
OUTPUT ACTIV		(SADOT)	ଡ.ଡ଼ଡ	ตุ๋ลด	86, ØN
DUTPUT ACTIV	E FROM MRD	(TDOA3)	54.0N	48.0N	28,0N
OUTPUT HOLD	FROM CS1	(TDOH1)	300.N	3ตต_่ี N	24,0N 22,0N
OUTPUT HOLD		(SHOUT)	300 N	300, N	55, DN
DUTPUT HOLD		(TDOH3)	138.N	116.N	34,0N
סטידפטי אטנס		(TPDH)	136 _s N	112 N	34.QN
READ CYCLE T		(TRC)	272.N	232,N	128.N
WRITE CYCLE	TIME	(TWC)	208.N	184.N	128 N
IIL	IIH		VIC1	VICE	
A0 -209,	NA 51.	SNA ·	3.95 V	ლ3,06 V	
A1 -267.			3 12 V	-3-11 V	
A2 +152.		LNA	3.12 V	•3,14 V	
A3 =115.	NA 36.	5 N A	3.13 V	93,14 V -3,13 V	
A4 =102 a			3.15 V	-3,16 V	
A5 ≈50,2			3_05 V	y3,t2 V	
A6 =41.1			3_08 V	-3,11 V	
A7 -35.8	NA 42,	INA	3.09 V	-3.12 V	
CS1 #32,6			3,12 V	-3,12 V -3,14 V -3,07 V -3,10 V	
CS2 -40.5			3.14 V	+3,14 V	
MWR =77,9			3.07 V	-3,07 V	
MRD =46,4	NA 41.	7 N A	3.11 V	-3,10 V	
D10 +33,3			3,20 V	±3,16 V	
DI1 -32,7			3.17 V	+3,14 V	
DI2 -35,8			3.19 V	-3,16 V	
DI3 =37.5	NA 44.1	SN A	3.19 V	-3.13 V	

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RÇA	CDP1822SD	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP:	85 C SN:	3
					PAGE	8 OF 10	
	ממת	001	500	003			
VOLI	125.MY	130.MV	135.MV	135, MV			
V01.2	125.MV	140.MV	155.MV	150.MV			
VOH1	4.82 V		4.82 V	4,82 V			
AOHS	9.75 V	4,82 V 9,75 V	9.74 V	9,76 V			
IDNS	5.95MA	5.65MA	5.35MA	5.45MA			
IDNS	14,9MA	13,6MA	12.2MA	17.6MA			
TUP	-2.27MA	-2.24MA	-2.24MA	#2,29MA			
IDP2	■4,98MA	-4.97MA	-4.85MA	#5.06MA			
rozi	10,2401	10,2UA	10,2UA	10,2UA			
IOZZ	-74. ONA	-75.2NA	-78,3NA	-75,7NA			
IOZ3	10,2UA	10.2UA	10,2UA	10.204			
1024	₩74 _₩ 7NΛ	-78,3NA	-78.2NA	-77 3NA			
1025	AUS,01-	-10,2UA	~10,2UA	mim. 2UA			
1076	=54.8NA	-75.0NA	-65_8NA	#78, ØNΔ			
1027	-44,3NA	-57.5NA	-50.7NA	±73,5NA			
IOZ8	-65,6NA	-80,7NA	-73.0NA	₩81.9NA			
TLOP	260.UA						
T	tentre at the late of						
ILI	-35,0UA						
ILS	-50.0UA						
IL3	-35,0UA						
IL4	=35,0UA						
1 F o	±33°ผกัช						

สุ . i. อน PASSED GALPAT (WIDE LIMITS) VCC=10V PASSED GALPAT (TIGHT LIMITS) VCC=10V PASSED GALPAT (TIGHT LIMITS) VCC=5V

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FAILED DATA RETENTION	TEST ADD =	16 DTAG :	ø PINI	017
	VCC	= 4.5V	5.ev	10.0V
ADDRESS ACCESS TIME	(TAA)	560 N	220 N	100.N
DATA SETUP TIME DATA HOLD TIME	(TDS) (TDH)	18,0N 16.0N	16.0N	8.00N 14.0N
ADDRESS SETUP TIME	(TAS1)	4.00N	4 ๋. ตุดุท	4.00N
ADDRESS SETUP TIME	(TAS2)	124 N	104.N	56, ØN
ADDRESS HOLD TIME WRITE PULSE WIDTH	(TAH) (TWP)	-16,0N 76,0N	÷12.0N 68.0N	-4,00N 40,0N
Mante George Mante	(111.)	102014		
CS1 SETUP TIME	(TCSS1)	0 . NO	ស្គ ស្គ	70,0N
CS2 SETUP TIME	(TCSS2)	0.00	<i>ភ</i> ុខ៧	66,0N 14,0N
CS1 HOLD TIME	(TCSH1)	0.00	ଜ୍ଜଣ	14,0N
CS2 HOLD TIME	(TCSH2)	u • QQ	«± pd	14.0N
OUTPUT ACTIVE FROM CS	1 (TDGA1)	0.00	ଉ', ଉମ	98 ู่ ØN
OUTPUT ACTIVE FROM CS.		ด.ผูต	ด์ ติด	98, ØN
OUTPUT ACTIVE FROM MR	D (TDOA3)	58.ØN	50.0N	30.0N
OUTPUT HOLD FROM CS1	7400845	700 N	300, N	28, ØN
OUTPUT HOLD FROM CS2	(TDOH1) (TDOH2)	300.N 300.N	300 N	26,0N
OUTPUT HOLD FROM MRD	(TDOH3)	138.N	116,N	36,00
OUTPUT HOLD FROM MWR	(трон)	136.N	112,N	36, ØN
READ CYCLE TIME	(TRC)	280 N	248 N	136.N
WRITE CYCLE TIME	(TWC)	224 _* N	200.N	128.N
IIL	IIH	VICI	VICS	
A0 #1,23UA	284 NA	3.04 V	=3,04 V	
A1 w1.19UA	277 NA	3.10 V	-3,10 V	
A2 #963.NA	ANA DES	3.11 V	-3,13 V -3,11 V	
A3 =741.NA	205.NA	3.12 V	#3'.11 V	
A4 =660.NA	201 NA	3.13 V	3,14 V	
	260,NA	3.03 V	-3,10 V -3,09 V -3.10 V	
A6 =236.NA	241, NA	3.06 V	-3,09 V	
A7 #205,NA	243.NA	3.07 V	-3.10 V	
CS1 =184.NA	277 NA	3.10 V	-3,11 V	
CS2 -240.NA	277, NA 271, NA	3.13 V	±3,13 V	
MWR #440 NA	204 NA	3.05 V	#3,13 V #3,05 V #3,09 V	
MRD =265.NA	235.NA	3.09 V	-3.09 V	
DIØ =190.NA	257,NA	3.18 V	#3 15 V	
	255, NA	3,15 V	53,15 V 53,13 V 53,15 V	
	260 NA	3,18 V	#3,15 V	
DI3 =211.NA	256 NA	3.17 V	~3.12 V	
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C	٨	GE		1	7 (n	F	4	<i>(</i> 2)	
-بو	ж	La C	j.	L Ł	, I	IJ.	,	_ 1	v.	

	000	001	002	200
VOL1 VOL2 VOH1 VOH2	135.MV 145.MV 4.80 V 9.72 V	145.MV 155.MV 4.80 V 9.72 V	155.MV 175.MV 4.80 V 9.71 V	150, MV 170, MV 4, 81 V 9,72 V
IDN1 IDN2 IDP1 IDP2	5.35MA 13.3MA ~2.05MA ~4.47MA	5.10MA 12.2MA -2.04MA -4.47MA	4.85MA 10.9MA -2.00MA -4.32MA	4.90MA 11.3MA -2.07MA -4.56MA
IUZ1 IUZ2 IUZ3 IUZ4	10,2UA -813,NA 10,2UA ANS,NA	10.7UA -791.NA 10.2UA	10'.2UA -787.NA 10.2UA -774.NA	10.2UA =761.NA 10.2UA =773.NA
1025 1026 1027 1028	-10.2UA -788.NA -584.NA -804.NA	-10.2UA -774.NA -589.NA -802.NA	-10,2UA -771.NA -573.NA -783.NA	-10.2UA -752.NA -640.NA -759.NA
ILDP	350 _e UA			
IL1 IL2 IL3 IL4	-165,UA -220,UA -130,UA -115,UA			

RCA	CDP1822SD	256 X 4	CMOS	STATIC RAM	31	AUG 78	TEMP:	25 C	SNI	33
							PAGE	1 OF	10	

PASSEU	GALPAT GALPAT GALPAT	CTIGHT	LIMITS) LIMITS) LIMITS)	VCC=10V	REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR
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PASSED DATA RETENTION TEST

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	· PHIA GEORGIA	3.7 120,	• •		
	U	vo	C = 4.5V	5 . øv	10'.0V
AUDRES	SS ACCESS TIME	(TAA)	200 N	175.N	80.0N
	SETUP TIME	(TDS)			
	IDLD TIME		24,ØN	18.ØN	8 pon
AUIV I	11/2 TANE	(TDH)	10.0N	10.0N	12.0N
ADDRES	SS SETUP TIME	(TAS1)	ia, øn	8.00N	4.00N
	S SETUP TIME	(TAS2)	96, ØN	84. QN	42.0N
	S HOLD TIME	(TAH)	=16,0N	-12.AN	-2.00N
	PULSE WINTH	(TWP)	70.0N	62.0N	36 .0N
	Manager of the State	*******	1.01	Dr # wile	_
	SETUP TIME	(TCSSI)	150 N	130, N	68,000 64,000 24,000 22.00
CS2 S	SETUP TIME	(TCSS2)	146.N	156 N	64. UN
CS1 F	IOLD TIME	(TCSH1)	46, ØN	40.0N	24 an
CS2 H	HOLD TIME	(TCSH2)	46.0N	40.0N	22 MN
	-				
QUTPUT	ACTIVE FROM C	S1 (TDOAI)	196.N	172,N	88 ØN
րկԳրկն	ACTIVE FROM C	(SAOOT) SE	194 N	168.N	86,0N
OUTPUT	ACTIVE FROM M	IRD (TDOA3)	46.0N	42.0N	26.ØN
		_			
0UTP U1	HOLD FROM CS:	(TDOH1)	132.N	102,N	22, 0N
#####################################	HOLD FROM CS2	(SHOOT)	128 N	100 N	22 AN
OUTPUT	'HOLD FROM MRD	(TDOH3)	132.N	110,N	30,0N
	' HOLD FROM MUR		124.N	106, N	30.0N
	YCLE TIME	(TRC)	216.N	192,N	120.N
	CYCLE TIME	(TWC)	208.N	176.N	112.N
	., -, -, -, -, -, -, -, -, -, -, -, -, -,	(14-20)	LEW # 14	110411	114 14
	IIL	IIH	VIC1	Aics	
ΑØ	≈1.8gNA	1,80NA	2.96 V	-2,93 V	
A1	=1,60NA	2,60NA	2.97 V	#3.01 V	
A2	#2,10NA	1.80NA	2.97 V	-3,01 V -3,00 V	
A3	-3,00NA	1.80NA	2.98 V	#2.99 V	
A 4	91.7ØNA	1,60NA	3.02 V	-3,05 V	
AS	⇒1.50NA	1.90NA	2,94 V	-2.97 V	
A 6	-2.10NA	1,60NA	2,96 V	-2,98 V	
A 7	-2.00NA	1 90NA	2.97 V	-2,97 V -2,98 V -3,00 V	
	.				
CS1	#2.10NA	1,50NA	3.71 V	-3-00 V	
csz	#1 # 90NA	1,70NA	3,01 V	-3,04 V	
MWR	=2.10NA	2,00NA	2,96 V	#2,98 V	
MRD	#1.60NA	1.80NA	3,00 V	=2.99 V	
DIØ	- 2 (A(A)) A	4 70NA	7 40 11	" og *	
	₩2.00NA	1,70NA	3.09 V	-3,02 V	
DII	#1,90NA	1,60NA	3.05 V	-2,99 V	
012	=4.30NA	1,90NA	3.09 V	-3.02 V -3.03 V	
013	-1.90NA	1.70NA	3.07 V	-3.03 V	

RCA	CDP1822SD	256 X 4 CMDS	STATIC RAM	31 AUG 78 TE	MP:	as c sn	i 33
				P	AGE	2 OF 10	
	non	001	pož	003			
VOL 1	90,0MV	VMQ.Ze	100.MV	100, MV			
ADLS	100.MV	110.MV	125.MV	120.HV			
ADHI	4.86 V	4,86 V	4,85 V	4,86 V			
ADHS	9 80 V	9.80 V	9,78 V	9 8		Ťi.	
ION1	8.25MA	7.85MA	7_25MA	7 40MA			
IDN2	19.2MA	17,4MA	15.3MA	15.8MA			
IDP1	-2,74MA	-2,75MA	=2.65MA	-2,77MA			
1065	#5.99MA	-6.02MA	- +5,74MA	⇔6,08MA			
1021	16.9NA	19,9NA	15,7NA	SW"SNY			
IOZZ	19.7NA	16.9NA	18,6NA	17_@NA			
1023	15,7NA	19,9NA	16,7NA	17,7NA			
1074	14.2NA	22,3NA	14.1NA	21,2NA			
1025	21.3NA	15.5NA	20,7NA	16,0NA			
1026	21,3NA	15.8NA	20,5NA	15,8NA			
1027	21,3NA	15,5NA	20,0NA	15,8NA			
1028	20.8NV	16.1NA	19.9NA	16 0NA			
71 B.D	E gove						
ILDP	⇔5.00UA						

-5.00UA -5.00UA -5.00UA

IL1 IL2 IL3 IL4 :- i ::- i

RCA	CDP18225D	256 X 4	CMOS STATIC	RAM 31	AUG 78	TEMP:	-20 C SN:	33
						PAGE	3 OF 10	

PASSED	GALPAT	(WIDE	LIMITS)	VCC=1ØV	
PASSED PASSED			LIMITS)	VCC=10V VCC=5V	REPRODUCIBILITY OF THE ORIGINAL PAGE IS FOOR

PASSED DATA RETENTION	N TEST			
	vçc	* 4,5V	5', ØV	10.0v
ADDRESS ACCESS TIME	(AAT)	195.N	170 N	70.0N
DATA SETUP TIME	irosi	24.0N	18.0N	8.00N
DATA HOLD TIME	(TĎH)	8,00N	8.00N	10.0N
ONTH HARD TRUE	2,0,		Ç M SI WIY	* 10 # 19.11
ADDRESS SETUP TIME	(LEAT)	16,0N	12.0N	4.pgn
ADDRESS SETUP TIME	(TAS2)	94 , ØN	80. NN	38,0N
ADDRESS HOLD TIME	(TAH)	=14 ืØN	-12.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	72.ØN	62.MN	34.0N
			,	
CS1 SETUP TIME	(TCSS1)	144.N	124, N	. 65° 0N
CS2 SETUP TIME	(TCSS2)	142.N	150"N	60,0N
CS1 HOLD TIME	(TCSH1)	40, ØN	34.0N	22,00
CS2 HOLD TIME	(TCSH2)	42 @N	36.ØN	55.0N
			7	
	\$1 (TDOA1)	190.N	160' N	84, ØN
	S2 (TDOA2)	186.N	158 N	82,00
OUTPUT ACTIVE FROM ME	RD (TDOA3)	42.0N	38,0N	55.QN
OUTPUT HOLD FROM CS1	(TDOH1)	124.N	94.ØN	18,00
OUTPUT HOLD FROM CSE	(TD0H2)	122 N	94. ØN	20 0M
OUTPUT HOLD FROM MRD	(TDOH3)	128 N		20,0N
OUTPUT HOLD FROM MWR	(TPDH)	124.N	108 N	28,0N 30,0N
READ CYCLE TIME	(TRC)	208*N	1 40 N	144.N
WRITE CYCLE TIME	(TWC)	224.N	176' N 184 N	96.0N
Marie Olome Itue	Cinci	CET # 14	¥ th d ■ lA	الق ق ال
III	IIH	VIC1	AICS	
AØ #200.PA	200 PA	3.01 V	#2'98 V	
A1 -200 PA	600,PA	3.03 V	#2,98 V =3,06 V	
A2 +300.PA	200 PA	3.02 V	-3,05 V	
A3 #700.PA	200 PA	3.03 V	#3,04 V	
**************************************	ATT TO THE TOTAL PROPERTY OF THE TOTAL PROPE	36/2 ,		
A4 =300.PA	200 PA	3.07 V	-3.10 V	
A5 -200.PA	300,PA	3.00 V	#3,02 V	
A6 =300,PA	200, PA	3,01 V	-3,03 V	
A7 -400 PA	300.PA	3.02 V	-3.05 V	
	•			
CS1 =300,PA	200, PA	3'.06 V	±3,05 V	
CS2 #300.PA	200, PA	3,06 V .	≈3,10 V	
MWR -300.PA	300,PA	3.01 V	#3,03 V	
MRD =200.PA	300.PA	3,05 V	#3.04 V	
DIØ #300.PA	300 . PA	3.13 V	÷3,08 V	
DI1 =400.PA	200, PA	3.11 V	-3,04 V	
DI2 P1.50NA	400 PA	3.13 V		
D13 =300.PA	300.PA	3.12 V	-3,08 V -3,08 V	
ひょき きつりりょだい	コログラにお	-7 = 1 E V	A & A & A	

RCA	COP18228D	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP	-20 C	SNI	33
					PÄGE	4 OF	10	
	מסמ	001	200	200				
VOL2 VOL2 VOL1	75.0MV 85.0MV 4.88 V 9.82 V	80,0MV 95.0MV 4.88 V 9.83 V	90.0MV 105.MV 4.88 V 9.82 V	85.0MV 105.MV 4.88 V 9.82 V				
IDN1 IDN2 IDP1 IDP2	9.35MA 22.0MA -3.2MA -6.98MA	8.90MA 20.0MA -3.23MA -7.05MA	8.25MA 17.7MA -3.14MA -6.73MA	8,40MA 18,3MA -3,25MA -7,09MA				
1071 1072 1073 1074	2.60NA 300.PA 7.4UNA 5.60MA	4,90NA 7.70NA 500.PA 900.PA	2.90NA =100,PA 6.20NA 5.90NA	3,00NA 6,40NA 800,PA -100.PA				
1025 1026 1027 1028	500.PA 800.PA 500.PA 800.PA	6.60NA 6.80NA 6.70NA 6.70NA	-200,PA -300,PA -300,PA -500.PA	6,80NA 6,60NA 6,80NA 6.70NA				
ILDP	=10.0UA			•				
IL1 IL2 IL3 IL4	-5.00UA -5.00UA -5.00UA -5.00UA							

RCA	CDP1822SD	256 X	4 cmos	STATIC RAM	31 AUG 78	темрі	≃55 C SN	: 37
						PAGF	5 OF 10	1 2 1
PASS	EO GALPAT EO GALPAT ED GALPAT	(TIGHT	LIMITS) LIMITS) LIMITS)	VCC=10V VCC=10V VCC=5V				

	vcc	= 4.5V	5.0V	10.0V
ADDRESS ACCESS TYME DATA SETUP TIME DATA HOLD TIME	(TAA) (TDS) (TDH)	195.N 30.0N 8.00N	160.N 22.0N 8.00N	65.0N 8.00N 10.0N
ADDRESS SETUP TIME ADDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WIDTH	(TAS1) (TAS2) (TAH) (TWP)	14,0N 90,0N -14,0N 70,0N	10.0N 74.0N H12.0N 64.0N	4 .00N 34 .0N =2 .00N 32 .0N
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS1) (TCSS2) (TCSH1) (TCSH2)	142.N 152.N 40.0N 28.0N	116,N 128,N 36,MN 20,MN	52,0N 62,0N 12,0N
OUTPUT ACTIVE FROM CS OUTPUT ACTIVE FROM CS OUTPUT ACTIVE FROM MR	(SADOT) S	186 "N 196 "N 38 "ØN	154, N 164. N 34, MN	86,0N 86,0N 80,0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH1) (TDOH2) (TDOH3) (TPOH) (TRC) (TWC)	118.N 140.N 126.N 122.N 200.N 208.N	90.00 110/0 106/0 102/0 176/0 160/0	18,0N 20,0N 28,0N 28,0N 104.N 96.0N
IIL	IIH	VIC1	V1C2	
A1 0.00 A A2 =100.PA	0.00 A 200.PA 100.PA 100.PA	3.06 V 3.09 V 3.08 V 3.10 V	-3.04 V -3.13 V -3.12 V -3.10 V	
A5 0.00 A A6 0.00 A	0.00 A 100.PA 100.PA 100.PA	3.13 V 3.06 V 3.08 V 3.08 V	#3,15 V #3,09 V #3,10 V #3,12 V	
CS2 =100.PA MWR =100.PA	0.00 A 100.PA 100.PA 100.PA	3.13 V 3,13 V 3.08 V 3.12 V	73,17 V -3,15 V -3,10 V -3,11 V	
DI1 0,00 A	100.PA 100.PA 100.PA 100.PA	3,18 V 3,16 V 3,19 V 3,18 V	-3,13 V -3,10 V -3,13 V -3,13 V	

RCA	CDP1822SD	256	X	4	CMOS	STATIC	RAM	31	AUG	78	TEMP:	=55	C	\$N:	33
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PA	GF	6	n F	1 (7)

	DDØ	001	200	Ead
VOL:	70.0MV	75.0MV	80,0MV	80.0MV
	75.0MV	85.0MV	95,0MV	90.0MV
A0H5	4.89 V	4,90 V	4.89 V	4,90 V
A0H1	9.85 V	9,85 V	9.84 V	9.85 V
IDN1 IDN2 IDP1	10,4MA 24,8MA -3,73MA	9',90MA 27.7MA	9.25MA 20.2MA	9.40MA 20.8MA
IDP2	#8.Ω3MΛ	₩3,79MA ₩8,23MA	#3,67MA #7,83MA	#3,79MA AMNS,8≈
1021	#600.PA	5.30NA	≈1.80NA	5,40NA
	2.20NA	2.10NA	400.PA	2.80NA
1023	2.10NA	700.PA	2.50NA	-100.PA
	-1.20NA	4.70NA	-1.00NA	4.00NA
1075	4.70NA	-700,PA	3,70NA	100, PA
1076	5.20NA	-800,PA	3,60NA	-200, PA
1027	5.10NA	-9001PA	4.10NA	=300°PA
	5,60NA	-1.10NA	4.10NA	=500°PA
ILDP	⇔5.00UA			
IT3 IT3 IT1	#5.00UA #5.00UA #5.00UA			
I L, 4	⇔5,00UA			

RCA	CDP18225D	256 X 4	CMOS STATIC F	RAM 31 AUG 78	TEMPÍ	85 C	SN:	33

PAGE T OF 10

PASSED GALPAT (WIDE LIMITS) PASSED GALPAT (TIGHT LIMITS) PASSED GALPAT (TIGHT LIMITS)	Unn-enu	REPRODUCIBILITY OF THE ORIGINAL PAGE IS FOOR
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. MADED BAIN WEITHIED	120;			
	VCC	= 4,5V	5.øv	10,0V
ADDRESS ACCESS TIME	(TAA)	205.N	180'N	85 ' .0N
DATA SETUP TIME	(TDS)	24, ØN	50,0N	8 00N
DATA HOLD TIME	(TDH)	12.0N	12.0N	14 0N
	.	× = # 0 · ·	# er 30 daza	A
ADDRESS SETUP TIME	(TAS1)	8.00N	8.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	104.N	94.7N	48,0M
ADDRESS HOLD TIME	(TAH)	+18, ØN	-14.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	80°, 0N	70.0N	42.0N
		•		
CS1 SETUP TIME	(TCSS1)	158 a N	138,N	74, ØN
CS2 SETUP TIME	(TCSS2)	154.N	134.N	70,0N
CS1 HOLD TIME	(TCSH1)	54,0N	46.0N	30,0N
CS2 HOLD TIME	(TCSH2)	56.ØN	48.0N	58,0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	208.N	184,N	98, ØK
OUTPUT ACTIVE FROM CS2	(SAOUT)	204.N	180.N	58,0N 96,0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	50.0N	46.ON	58.0N
BURBLE US. B. BUSSI S.S.		1_1	F .	
OUTPUT HOLD FROM CS1	(TDOH1)	136 N	106 N	24, ØN
OUTPUT HOLD FROM CS2	(SHOOT)	132.N	104, N	26,0N 34,0N 34,0N
OUTPUT HOLD FROM MRD	(TDOH3)	134.N	112, N	34,0N
OUTPUT HOLD FROM MWR	(TPOH)	128.N	108 N	34.0N
READ CYCLE TIME	(TRC)	224.N	200 N	128.N
WRITE CYCLE TIME	(TWC)	216 N	184.N	120.N
IIL II	IH	VICI	VICE	
	5,4NA ·	2,94 V	-2,91 V	
	7.3NA	2.96 V	#3,00 V	
	5.5NA	2.96 V	-2,99 V	
S 48.88 EA	4 " 9 N A	2.97 V	⇔2.98 V	
A4124 4314 24	(I (CEN) 4	7 55 4	· **	
• ·	4.ONA	3.00 V	-3,04 V	
-	5,8NA 5 7NA	2,93 V	-2,95 V	
	5,3NA 5,6NA	2.95 V	-2,96 V	
AL SEG# 2144 E	A WIND & C	2.96 V	=2,99 V	
CS1 -25,9NA 23	5,1NA	2.99 V	<u>.</u> 2,99 V	
	4.3NA	2,99 V	-3,03 V	
***	4.5NA	2,94 V	=2,96 V	
	4.1NA	2.98 V	-2.98 V	
	4.6NA	3,08 V	⊕3,01 V	
	4.INA	3,04 V	-2,97 V	
	4.8NA	3,07 V	+3,01 V	
DI3 =23.8NA 24	4.INA	3.05 V	~3.01 V	

RCA	CDP182280	256 X 4 CMOS	STATIC RAM	31 AUG 78	темр:	85 C	SN:	33
					PAGE	A OF	10	
	Dog	001	500	200				
VOL 1	105.MV	110 HV	120.MV	115, MV				
VOL 2	115.MV	130 MV	150.MV	145.MV				
VDH1	4.83 V	4,83 V	4.82 V	4,83 V				
VOHS	9.76 V	9.76 V	9.74 V	9,76 V				
IDNI	7.10MA	6.70MA	6 <u>- 5</u> 0MV	6,35MA				
IDNS	16.3MA	14.8MA	AMD.E1	13.5MA				
IOP1	AM1E.S-	-2,31MA	42,22MA	-2,34MA				•
1065	₩5.05MA	-5.08MA	94.82MA	-5.16MA				
1071	151.NA	158,NA	151.NA	147 tea				
1072	155.NA	150,NA	156.NA	147.NA				
1023	151.NA	153.NA	153.NA	146 NA				
1024	158,NA	147.NA	154.NA	150.NA				
1025	156.NA	152.NA	159.NA	152, NA				
1 026	160.NA	156,NA	147.NA	160,NA				
IUZ7	150 NA	159.NA	150 NA	148,NA				
1028	159 NA	150.NA	154.NA	153.NA				

ILDP	=5,00UA
ILi	=20.0HA
IL2	480.0UA
IL3	AUN.NS-
TLA	-20 WILL

RCA	CDP18223D	256 X 4	CMOS STATIC RAM	31 AUG 78	TEMP	125 C	SN:	33
								1

PAGE 9 0F 12

PASSED	GALPAT	(WIDE	LIMITS	VCC=1ØV
PASSED	GALPAT	(TIGHT	LIMITS)	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS	VCC=SV

PASSED DATA REYENTION TEST

	vcc	≈ 4,5V	5, ØV	ïø.av
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA) (TDS) (TDH)	220 N 24 0N 14 0N	195 N 20 M 14 ON	95,0N 8,00N 14,0N
ADDRESS SETUP TIME ADDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WINTH	(TAS1) (TAS2) (TAH) (TWP)	6.70N 114.N -18,2N 84.0N	6.00N 104.N -16.0N 76.0N	4.00 56.00 44.00 44.00
CS: SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TC8S1) (TC892) (TC8H1) (TC9H2)	166 N 162 N 54 ON 56 ON	146, N 142. N 48, MN 50, MN	80,0N 78,0N 30,0N 30,0N
OUTPUT ACTIVE FROM CS: OUTPUT ACTIVE FROM CS: OUTPUT ACTIVE FROM MRI	(SACOT)	224 n 220 n 54 on	200, N 196.N 50.0N	106.N 106.N 30.0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRD OUTPUT HOLD FROM MWR OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH1) (TDOH2) (TDOH3) (TPOH) (TRC) (TWC)	140.N 138.N 134.N 130.N 240.N 240.N	110 N 108 N 114 N 110 N 216 N 200 N	38,00 36,00 36,00 38,00 128,0 128,0
IIL :	TH	VIC1	AICS	. •
AZ w154 NA	150, NA 153, NA 148, NA 147, NA	2.95 V 2.97 V 2.96 V 2.98 V	÷2,91 V •3,00 V •3,00 V •2,99 V	
A5 0151 NA 1 A6 0155 NA	141, NA 148, NA 148, NA 149, NA	3.01 V 2.94 V 2.95 V 2.97 V	-3,05 V -2,95 V -2,97 V -3,00 V	
C82 #142.NA :	137, NA 141, NA 140, NA 138, NA	3.00 V 3.00 V 2.95 V 2.99 V	-2,99 V -3,04 V -2,97 V -2,99 V	
DI1 =144.NA :	144, NA 143, NA 141, NA 138, NA	3.09 V 3.05 V 3.08 V 3.06 V	3,02 V 32,08 V 3,08 V 3,08 V	

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RÇA	CDP1822SD	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMPI	125 C	SN:	3`
					PAGE	10 OF	10	
	DOB	pat	005	003				
VQL 1	115.MV	125,MV	135.MV	130° MV				
vor5	130 MY	145 MV	170 MV	160 MV				
VOHI	4,81 V	4,81 V	4.80 V	4.81 V				
VOH2	9.72 V	9.72 y	9.71 V	4,81 V 9,72 V				
IDN1	6.30MA	5' 95MA	5.55MA	5,65MA				
IDN2	14.4MA	13.1MA	11.5MA	11,9MA				
IDP1	-2.07MA	-2.07MA	AMSD.S.	-2,10MA				
1065	4. 52MA	-4.55MA	-4.34MA	#4-61MA				
IOZ1	643.NA	621,NA	612.NA	695, NA				
IOZ2	643,NA	614, NA	606,NA	607, NA				
1023	637 NA	611 NA	609,NA	606.NA				
IOZ4	642.NA	612,NA	600.NA	611_NA				
1025	649.NA	621, NA	621 .NA	624, NA				
1026	543.NA	627,NA	603.NA	617, NA				
1027	635 NA	621.NA	609.NA	606,NA				
1028	645 , NA	616.NA	608.NA	615 NA				
ilop	40,0UA							
	THE SHOPE							
IL 1	-90.0UA							
ILE	-105.UA							
IL3	-85,0UA							
YL 4	-70.QUA							
4 Sp. 77	‱.ស⊽សុ∏¥(

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RCA	CDP18228D	256 X 4	CMOS STATIC RAM	31 AUG 78	TEMP	25 C 3N:	34
					DAGE	1 85 18	

PASSED	GALPAT	(WIDE	LIMITS)	VÇC=10V
PASSED	GALPAT	CTIGHT	LIMITS)	VCC=10V
PASSED	GALPAT	(TIGHT	LIMITS)	VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

MOOTO DAIN WEITHING	401			
	VCC	= 4.57	5 . ØV	10.0V
ADDRESS ACCESS TIME	(TAA)	27Ø.N	220.1	85.0N
DATA SETUP TIME	(TDS)	24, ØN	18,0N	8 . RØN
DATA HOLD TIME	(TĎĤ)	10.0N	10.0N	12.00
SHIN HOUGH TENE	(10)	1010.	The second section	
ADDRESS SETUP TIME	(TAS1)	14,0N	12.ªN	4.00N
ADDRESS SETUP TIME	(TAS2)	134.N	110.N	48 ØN
ADDRESS HOLD TIME	(TAH)	#18,0N	=14.0N	=4.00N
WRITE PULSE WIDTH	(TWP)	72.ØN	62.0N	38.0N
	• • • • •			
CS1 SETUP TIME	(TCSS1)	164 N	140 N	70,0N
CS2 SETUP TIME	(TCSS2)	160 N	138.N	68 0N
CS1 HOLD TIME	(TCSH1)	40,0N	36,0N	24, ØN
CS2 HOLD TIME	(TCSH2)	42.ØN	38.9N	22,0N
	* / ~ ~ ~			
OUTPUT ACTIVE FROM CS1	(TDOA1)	272.N	224, N	96, ØN
OUTPUT ACTIVE FROM CS2	(SAOUT)	27Ø.N	855 N	94, DN
OUTPUT ACTIVE FROM MRD	(TDOA3)	50.0N	44.0N	26.0N
The state of the s	*	41 Sp. 10 44		
OUTPUT HOLD FROM CS1	(TDOH1)	140 N	108 N	28, ØN
OUTPUT HOLD FROM CS2	(TDOH2)	136.N	196, N	28, DN
OUTPUT HOLD FROM MRD	(TDOH3)	134.N	112,N	34 0N
OUTPUT HOLD FROM MWR	(TPDH)	130,N	108 N	32.0N
READ CYCLE TIME	(TRC)	248.N	216,N	120.N
WRITE CYCLE TIME	(TWC)	256 N	184.N	112 N
	•	4	• • • •	
IIL II	Н	VIC1	AICS	
AØ #1.80NA 1.	40NA .	5"35 A	-2,91 V	
	90NA	2.98 V	#2,99 V	
	SONA	2,98 V	#3.00 V	
	90NA	2.98 V	-3,00 V -3,00 V	
		77 T		
A4 -1.70NA 1'.	60NA	2,99 V	-3,00 V -2,98 V	
A5 #1.80NA 1.	70NA	2,94 V	-2.98 V	
A6 #1,40NA 1,	BONA	2,94 V	-2,98 V	
A7 =2,10NA 1.	60NA	2.95 V	-2,99 V	
,				
CS1 #1.30NA 1,	50NA	2,98 V	-2,97 V	
	50NA	3.02 V	-2 99 V	
	40NA	2,96 V	#2,96 V	
	BONA	2.97 V	₩2.97 V	
DIO #2,10NA 1,	BONA	3 02 V	-2,99 V	
DII =2,00NA 2,	20NA	3.03 V	≈2,97 V	*
DI2 -1.80NA 1,	90NA	3,03 V	-3,01 V	
	BONA	3.01 V	-2.97 V	
		- · · · ·		

RCA	CDP1822SD	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMPÍ	25 C	SN:	34
					PAGE	2 OF	10	
	NGO	001	. 508	003				
AOH5 AOH1 AOF3	105.MV 110.MV 4.84 V 9.78 V	110.MV 120.MV 4.84 V 9.78 V	115.MV 135.MV 4.84 V 9.77 V	115, MV 130, MV 4,85 V 9,78 V				
IDN1 IUN2 IDP1 IDP2	7.05MA 17.3MA -2.51MA -5.59MA	6.70MA 15.8MA -2.54MA -5.62MA	6.30MA 14.1MA -2.48MA -5.43MA	6,45MA 14,6MA -2,55MA -5,68MA				
1021 1022 1023 1024	ANP,85 ANP,35 ANP,55 ANP,85	AN8.05 AN8.15 ANS.25 ANP.15	26,0NA 24,1NA 20,0NA 23,2NA	19,7NA 20,5NA 25,3NA 21,7NA				
1025 1026 1027 1028	23,0NA 23.6NA 22.8NA 22.7NA	25.1NA 24.5NA 24.9NA 24.3NA	21,5NA 21,5NA 21,5NA 21.ØNA	23.0NA 23.4NA 22.7NA 23.1NA				
ILDP	+10.0UA							
IL1 IL2 IL3 IL4	#30,0UA #35,0UA #85,0UA #80,0UA							

RCA	CDP1822SD 256	X 4 CMOS	STATIC RAM	31 AUG 78	YEMPi →20 C
					PAGE 3 OF 10
PASSE	D GALPAT (WIDE	LIMITS	VCC=10V		
PASSE	D GALPAT (TIGH	IT LIMITS)	VCC=10V		
PASSE	D GALPAT (TIGH	T LIMITS)	VCC=5V		
PASSE	D DATA PETENTIC	N TEST			
					,
		,	VCC = 4.5V	5.0V	10.0v
ADDRES	SS ACCESS TIME	(TAA)	290 N	2201	N 80'. ØN
	SETUP TIME	(TDS)	26'. ØN	20.0	N 8.º@N
DATA	HOLD TIME	(TDH)	8.00N	10.0	N 12.0N
	SS SETUP TIME	(TAS1	18.0N	14.0	N 4.80N
	SS SETUP TIME	(TASE		106.	N 42 ØN
	SS HOLD TIME PULSE WIDTH	(TAH) (TWP)	+16.0N 76.0N	=14_0 66_0	
******	- Dage Wastin	((,,,,	10.01		_
	SETUP TIME	(TCSS)		132,	N 64, an
	SETUP TIME HOLD TIME	(TCSS; (TCSH)		130. 34.0	
	HOLD TIME	(TCSH	· · · · · · · · · · · · · · · · · · ·	36.0	N 55. QN
CUTPU	T ACTIVE FROM C	. C. T. C. T. C. A. S.	(3 770 N	297	N 88, ØN
	T ACTIVE FROM C			282, 280,	ก 66,ยก N 86,ยก
	T ACTIVE FROM M		,	40.0	
OUTPU'	T HOLD FROM CS1	(TDOH:	() 132.N	102.	N 24, ØN
	r HOLD FROM CS2			98.0	N 24,0N
	r HOLD FROM MRD	·	-	98.0 110.	N 30,0N
	T HOLD FROM MWR CYCLE TIMF	(TPDH) (TRC)	126,N 232,N	196, 208,	N 30.0N N 112.N
	CYCLE TIME	(TWC)	240.N	176.	N 104.N
	IIL.	IIH	VIC1	VICS	
		_	, 10, 1		
AØ	-400 PA	200 PA	3.03 V	-3,02 V	
A1 A2	=500.PA =300.PA	500.PA 300.PA	3.09 V 3.09 V	±3,10 V ±3,11 V	
A3	-200.PA	300 PA	3.09 V	43.11 V	
A 4		700 DA	7 44 0	*2****	
A 5	#300.PA #400.PA	300,PA 300,PA	3.11 V 3.05 V	=3,11 V =3,10 V	
A6	-200 PA	200.PA	3,05 V	#5,09 V	
A7	≈500.PA	300 PA	3.06 V	-3,11 V	
CS1	-200 _s PA	300 PA	3,10 V	-3,09 V	•
CS2	≈300 mPA	300,PA	3.13 Y	-3,10 V	
MWR MRD	-300.PA -300.PA	200.PA 400.PA	3,07 V 3.08 V	=3,07 V =3,08 V	
	िच्चान्य ⊈र्माः				
DIØ	#400 PA	200.PA	3.13 V	-3,09 V -3,08 V	
011 012	⇔400.PA ⇔300.PA	500.PA 400.PA	3.14 V 3.14 V	=3,08 V +3,11 V	
013	-200.PA	300.PA	3.14 V	+3,11 V +3,08 V	
	•		D 226		

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SN:

RCA	CDP18228D	256	X	4	CMOS	STATIC	RAM	31	AUG	78	TEMP:	-20	C	SN:	34

PΛ	GF	4	OF	10

	ĐOØ	001	pos	D03
VOL1	90.0MV	95.ØMV	100.HV	100 MV
VOLS	95.0MV	105.MV	115.MV	110.MV
THOV	4 88 V	4 87 V	4.86 V	4,88 V
A0H5	9.81 V	9.81 V	9_81 V	9,82 V
10.15	7 10 2 4	/ .	7 . 7 . 1	
IDNI	7.95MA	7.60MA	7.20MA	7.30MA
INNS	19.9MA	18.3MA	16.4MA	17.0MA
TOP1	#2.99MA	-3,01MA	#2_94MA	17.0MA -3,04MA
IOP2	#6,58MA	-6.62MA	96.41MA	-6.73MA
	-			
IUZI	3.10NA	6,50NA	1.00NA	6,6MNA
IOZZ	6.00NA	3.00NA	4.20NA	3,30NA
1023	3.50NA	4.80NA	3.30NA	A MONA
IOZ4	1.30NA	7.90NA	400.PA	6.70NA
				<u>.</u>
1075	8.50NA	1,00NA	6.5UNA	1,30NA
I0Z6	8.20NA	1.00NA	6.90NA	1,00NA
1027	8,50NA	900.PA	6.7UNA	900,PA
1028	8.30NA	1.00NA	7.00NA	900 PA
ILDP	-10.0UA			
IL1	-25,0UA			
IL2	-30°0UV			
IL3	-70,0UA			
IL4	-70.0UA			

RCA	CDP1822SD	256 X 4	CMOS	STATIC	RAM	31	AUG	78	TEMP	#55 C	SN:	34
									PAGE	5 OF	10	

TT No.

·			PAGE	5 OF 10
PASSED GALPAT (TIGHT	r Limits) vo	C=10V C=10V C=5V	REPRODUCIBILI ORIGINAL PAGI	TY OF THE
PASSED DATA RETENTION	N TEST		•	
	vcc	= 4.5V	5 , Ø V	10 . 0V
ADDRESS ACCESS TIME DATA SETUP TIME DATA HOLD TIME	(TAA) (TDS) (TDH)	300 N 30 N 8 00 N	8.00K 8.00K 8.00K	75.0N 8.00N 10.0N
ADDRESS SETUP TIME ADDRESS SETUP TIME ADDRESS HOLD TIME WRITE PULSE WIOTH	(TAS1) (TAS2) (TAH) (TWF)	16.0N 132.N -18.0N -80.0N	10.9N 104.N -14.0N 66.0N	4.00N 38.0N -2.00N 32.0N
CS1 SETUP TIME CS2 SETUP TIME CS1 HOLD TIME CS2 HOLD TIME	(TCSS1) (TCSS2) (TCSH1) (TCSH2)	154.N 152.N 46.0N 46.0N	128 N 126 N 38 M 40 M	55.0N 58.0N 60.0N
OUTPUT ACTIVE FROM CS OUTPUT ACTIVE FROM CS OUTPUT ACTIVE FROM ME	(SAOOT) SE	294.N 292.N 42.UN	224 N 222 N 38 M	84,0N 82,0N 22,0N
OUTPUT HOLD FROM CS1 OUTPUT HOLD FROM MRO OUTPUT HOLD FROM MWR READ CYCLE TIME WRITE CYCLE TIME	(TDOH1) (TDOH2) (TDOH3) (TPOH) (TRC) (TWC)	126.N 124.N 130.N 126.N 216.N 200.N	94.0N 92.0N 108.N 104.N 184.N 168.N	20,0N 28,0N 28,0N 136.N 136.N
III.	IIH	VICi	VICE	
A0 = 100.PA A1 = 100.PA A2 = 100.PA A3 0.00 A	100,PA 100,PA 100,PA 100,PA	3.13 V 3.18 V 3.18 V 3.18 V	-3,12 V -3,19 V -3,19 V -3,20 V	
A4 ~100.PA A5 ~100.PA A6 ~100.PA A7 ~100.PA	100.PA 100.PA 100.PA 100.PA	3.19 V 3.14 V 3.15 V 3.15 V	#3,19 V #3,19 V #3,18 V #3,18 V	
CS1 0.00 A CS2 0.00 A MWR -100.PA MRD -100.PA	100, PA 100.PA 0.00 A 100.PA	3.19 V 3.22 V 3.16 V 3.17 V	23,18 V 23,18 V 23,16 V 23,17 V	
DIØ = 100.PA DII = 100.PA DI2 = 100.PA DI3 = 100.PA	100,PA 200,PA 100,PA 300.PA	3.23 V 3.23 V 3.24 V 3.22 V	#3,18 V #3,17 V #3,20 V #3,17 V	

RCA	CDP1822SD	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP	⇒55 C	SN:	34
					PAGE	6 OF	10	
	000	100	500	003				
VOL 1	85.0MV	85.0MV	95'_ØMV	90 0HV				
AOF5	85.0MV	90.0MV	100.MV	100.HV				
VOH1	4.89 V	4,89 V	4.88 V	100 hv 4 89 v				
ADHS	9,84 V	9,84 V	9.84 V	9.84 V				
IDN1	A.BOMA	8.40MA	7.95MA	8 10MA				
IDNS	AMS,55	20.5MA	18.5MA	19.0MA				
IDP1	-3.44MA	-3.49MA	≒3 ,42MA	-3,54MA				
1065	-7.57MA	-7.67MA	97.43MA	.7.79MA				
IOZi	≈ 600,PA	5,80NA	-1.40NA	19.0NA				
1025	900 # P A	3.40NA	-500 PA	8,50NA				
1023	3.60NA	-100.PA	3.80NA	3,40NA				
1024	Suu*by	3.50NA	400.PA	6.60NA				
1025	3.70NA	BMOPA	1.70NA	6,20NA				
TOZ6	3,40NA	700,PA	2.10NA	6,40NA				
1027	3.70NA	800.PA	1.70NA	6,40NA				
1078	3.30NA	700.PA	2.10NA	6.60NA				
ILOP	⇒2.80UA							
YL1	-25,0UA							
ILS	=30,0UA							
IL3	-65_0UA							
IL4	-65.0UA							
I 5., **	B 1 # 6: C 4							

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(Successive) (Substantia) (Substantia)

RCA (CDP1822 S D 256	X 4 CMOS ST	ATIC RAM	31 AUG 78	TEMP: 85 C	SN:
					PAGE 7 OF	i@
PASSED PASSED		T LIMITS) VI T LIMITS) VI	CC=10V CC=10V CC=5V	REPRODI ORIGINA	UCIBILITY OF THE L PAGE IS POOR	<u>.</u>
		VC	5 = 4.5V	5.0\	10,00	,
DATA S	S ACCESS TIME ETUP TIME OLD TIME	(TAA) (TDS) (TDH)	270 N 24,0N 12.0N	225. 20,0 12.0	4QQ_8 NI	l
ADDRES ADDRES	S SETUP TIME S SETUP TIME S HOLO TIME PULSE WIDTH	(TAS1) (TAS2) (TAH) (TWP)	8.00N 132.N -18.0N 84.0N	8.00 110. 16.0 72.0	.N 54.0N IN -4.00N	! !
CS2 S	ETUP TIME ETUP TIME OLD TIME	(TCSS1) (TCSS2) (TCSH1) (TCSH2)	170 N 166 N 54 ON 56 ON	148, 144, 46.0	N 76,0N N 74,0N IN 30,0N	1 1
0 01 PUT	ACTIVE FROM C	Si (TDGA1)	274.N 270.N 54.ØN	232, 230, 48,0	N 106 N 104 N	
OUTPUT OUTPUT OUTPUT READ C	HOLD FROM CS1 HOLD FROM CS2 HOLD FROM MRD HOLD FROM MWR YCLE TIME CYCLE TIME	(TDOH1) (TDOH2) (TDOH3) (TPDH) (TRC) (TWC)	146 N 142 N 134 N 132 N 256 N 232 N	114, 112, 114, 110, 274, 200.	N 32,0N N 34,0N N 36.0N N 128,N	 - -
	IIL	IIH	VICI	vics		
AØ A1 A2 A3	=17,7NA =18,2NA =17,9NA =16,9NA	18.8NA 20.3NA 17.9NA 19.2NA	2.87 V 2.93 V 2.93 V	#2,86 V #2,94 V #2,94 V #2,95 V		
A4 A5 A6 A7	#17,6NA #18,0NA #29,2NA #18,5NA	17.9NA 19.7NA 191.NA 19.8NA	2.94 V 2.89 V 2.89 V 2.89 V	-2,95 V -2,93 V -2,92 V		
CS1 CS2 MWR MRD	=17,5NA =17,3NA =17,1NA =17,3NA	18,7NA 18.4NA 17.2NA 19,2NA	2.93 V 2.96 V 2.91 V 2.92 V	-2,92 V -2,94 V -2,91 V		
DIØ DI1 DI2 DI3	+19,9NA +19,6NA -17,8NA +17,4NA	21.5NA 21.9NA 20.0NA 19.7NA	2.97 V 2.98 V 2.98 V 2.96 V	#2,93 V #2,93 V #2,95 V #2,95 V		
			T) 22m			

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RCA	CDP1822SD	256 X 4 CMOS	STATIC RAM	31 AUG 78	TEMP	85 C	SN:	34
					PAGE	8 OF	10	
	Dog	DOi	poa	003				
VOLi	120,MV	130 MV	135.MV	135, MV				
VOLE	130.MV	145_MV	160.MV	155 MV				
VOH1	4.82 V	4,82 V	4.81 V	4,82 V				
VOHS	9.73 V	9,73 V	9.72 V	4,82 V 9,74 V				
IUNI	6.05MA	5.75MA	5.40MA	5,50MA				
IDNS	14.6MA	13.4MA	11.9MA	12.4MA				
IDPI	-2.13MA	-2,14MA	⇒5°09MV	-2,17MA				
IDP2	=4,74MA	-4.75MA	-4.60MA	-4 83MA				
TOZI	832.NA	238,NA	AN, DSS	228, NA				
IOZE	44.55°	A4,EES	223.NA	220,NA				
1023	352°NV	237,NA	550 NA	253,04				
1074	225.NA	229,NA	225.NA	218.NA			e	
1025	226.NA	235, NA	227_NA	227, NA				
1026	236.NA	A4.855	888 NA	228,NA				
IOZ7	\$58 " NV	238,NA	219.NA	\$59°NY				
1028	227.NA	229.NA	AN BES	221.NA				
ILDP	4.80UA							
ILi	40° 011A							
ILS	⊶50,0UA							
IL3	#105.UA							
IL4	#100.UA							

APPENDIX C SCHMOO PLOTS

```
TAS
     VS. TWP
            (ADDRESS R21)
                    VCC = 5.00 V
                                 TAS
                           70
               30
                     50
WPW
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30
40
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                     * ********
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                  ********
70
               ************
80
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            **************
           ************
100
           **********
110
           ***************
120
           130
           ************
140
150
           *****************
           ***********
160
     vs. Iwp (ADDRESS RZ)
                    VCC = 5.00 V
   TAS
               30
                                 TA5
                           70
   -10
                     50
al P W
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                   ***********
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        ***********
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        ************
160
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```
VS. IMP (ADDRESS RZI) VCC = 10.0 V
  LAS
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             50
                     TAS
NF &
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      ***********
80
      90
      100
      **********
110
120
      **********
130
      **********
      ****************
140
150
      ****************
      150
   VS. TWP (ADDRESS RZ) VCC = 10.0 V
  LAS
             50
                 70
                      IAS
WPW
20
3 ()
       *********
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     ***********
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     *************
60
     *****
70
     80
     ************
90
     100
     ***********
110
     120
130
     **********
140
     *********
     150
     ***********
160
```

```
VS. IWP (ADDRESS RZI) VCC = 5.00 V
              -10
                       10
     -30
                                FAH
               1
WE'N
30
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                ********
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70
              * * * * * * * * * * * * *
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100
              *********
110
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120
              *********
130
              **********
140
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160
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170
              *******
180
              ********
         VS. TWP
                  (ADDRESS RZ) VCC = 5.00 V
     hAi
                    6.1
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                * * * * * * * * * * *
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e () =

```
(AUDRESS RZI) VCC = 10.0 \text{ V}
           VS. PWP
                         10
      -30
                ~10
                                     TAH
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                     ******
170
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180
                     ******
                     (ADDRESS RZ) VCC = 10.6 v
      PAH
           VS. INF
                         10
                -10
                                    Тан
WPW
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                     *****
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110
                      *****
120
130
140
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160
                      *****
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                      ******
180
                      *****
```

```
TUS
         vS. TwP
                (DATA RZI) VCC = 5.00 V
                            50
                                   TDS
TWP
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            ************
7 û
            ***********
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90
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100
            110
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120
            **********
     TDS
         VS. TWP
                (DATA RZ)
                        VCC =
                               5.00 V
             10
                    30
                            50
                                   TUS
TWP
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```

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```
ros
             (DATA RZI) VCC = 10.0 V
       VS. TWP
    -10
                                TUS
IWP
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           *************
51)
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          ***********
160
          **********
110
          **********
120
          **********
    LDS
        VS. TWP
              (DATA RZ)
                      VCC =
                            10.0 V
                         50
                                TUS
           10
                  30
TwP
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            **********
50
           **********
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           ************
70
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           120
```

```
TOH VS. INP
                 (DATA RZI) VCC = 5.00 V
                                      TOH
                     10
                              30
TWP
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                ******
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90
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100
              *************
110
120
         VS. TWP
                 (DATA RZ) VCC =
     TOH
                                5.00 V
                                      TOH
                     10
                              30
TWP
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110
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```

```
TOH
         VS. IMP
                 (DATA RZI) VCC = 10.0 \text{ V}
                      10
             -10
                              30
                                       TDH
IWP
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                  *********
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100
                    *********
110
                    *********
120
                    **********
     PDH
          VS. IWP
                  (DATA RZ) VCC = 10.0 V
                                       TDH
TWP
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4υ
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120
```

11.

	ICC	VS.	GACPE	TI	A E.		VCC	=	10.0V
	0	1	10	,	20			1	CC
CYCLE			,	•					
100.N						>			
200,N				*					
400.N			*						
800.N									
1.600		*							
3.200		4							
6.40U	*								
12.80	*								
25.6U	*								
51.20		*							
102.0		*							
205.U	*								
410.0	*								
819.U	*								

DEVICE PASSED ALL TESTS

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```
TAS VS. TWP (ADDRESS RZI) VCC = 5.00 V
            30
                    50
                          70
                               TAS
WEW
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         120
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150
         160
         ************
   TAS VS. TWP (AUDRESS RZ) VCC = 5.00 V
                    50
               30
                               TAS
wPa
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                      * * * *
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100
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110
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120
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130
140
        ***********
        ************
150
        ***********
160
```

```
TAS
     VS. TWP
          (ADDRESS RZI) VCC = 10.0 V
        10
             30
                  50
                            TAS
wPw
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          *********
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100
        ***********
       ***********
110
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        **********
130
        ***********
140
        ***********
150
       *************
160
        **********
  TAS
     VS. TWP
          (ADDRESS RZ)
                 VCC = 10.0 V
        10
             30
                            TAS
                  50
wPw
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         **********
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100
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110
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120
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130
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       140
150
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```

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160

```
TAH VS. TWP (ADDRESS RZI)
                                   VCC = 5.00 V
                      10
      -30
                -10
                                    TAH
WYW
3∪
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               *****
           VS. TWP
                     (ADDRESS RZ)
                                    VCC = 5.00 V
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                                    HA'J
WPW
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8.0
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170
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180
```

```
(ADDRESS RZI)
                                        VCC =
      PAH
                                                 10.0 V
            VS. TWP
                                         TAH
      -30
                  -10
                              10
WPW
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170
180
                                        VCC = 10.0 V
      LAH
            VS. TWP
                       (AUDRESS RZ)
                                         PAH
      -30
wPw
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170
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```

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

```
IDS VS. TWP (DATA RZI) VCC = 5.00 V
                          50
                                TDS
INP
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          ***********
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          **********
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          ***********
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          ***********
100
          ************
110
          *********
          *******
120
    TOS
        VS. IWP (DATA RZ) VCC = 5.00 V
                                 TUS
           10
                          50
                   30
TwP
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                *********
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               **********
100
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110
               **********
```

```
TUS
        VS. THP (DAPA RZ1) VCC = 10.0 \text{ V}
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           10
                  30
                        50
                               TDS
THE
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          *******
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          *******
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          *******
70
          ********
80
90
100
          *************
110
         **************
120
          **************
    TUS
        VS. PWP
              (DATA RZ) VCC = 10.0 V
           10
    -10
                        50
                               TOS
TWP
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            ********
50
            *************
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           *********
70
           ************
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           *************
100
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110
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120
           ********
```

11.5

```
IDH VS. TWP
                     (DAPA RZI) VCC = 5.00 V
     = 30
               □ 1 U
                          10
                                    30
                                             TDH
TWP
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                      * * * * * * * * * * * * * * * * *
90
100
                     ***********
110
                     **********
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                     **********
      TUH
           VS. IWP
                     (DAIA RZ) VCC = 5.00 \text{ V}
                          10
               -10
                                   30
                                             TDH.
IWP
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```

4.4

```
TUH
           VS. TWP
                     (DATA RZI)
                                    VCC = 10.0 V
                -10
                            10
                                                TOH
Twp
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 90
100
110
                         **********
120
       TOH
            VS. TWP
                      (DATA RZ) VCC = 10.0 \text{ V}
      -30
                -10
                                      30
                                                TOH
                            10
TwP
30
 40
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110
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120
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```

RCA CDP1822SU 256 X 4 CMUS STATIC RAM 08 MAY 79 TEMP: 25 C SN: 2

	icc	٧S,	CACPE	T I	ME		VCC	=	10.07
	0	;	10	1	20			ī	cc .
CYCLE	••	·	•	•	•				
100.N						>			
200 . N				*					
400 N		•	*						
800 . N		*							
1.60U		*							
3.200		‡							
6.400	*								
12.8U		*							
25.6U	*								
51.20		+							
102.0		#							
205.U	*						•		
410.0	*								
819.U	*								

DEVICE PASSED ALL TESTS

```
TAS VS. TWP
             (ADDRESS RZI)
                     VCC = 5.00 V
         10
                30
                      50
                                  TAS
                            70
WPW
20
30
4υ
50
60
70
 80
 90
              *********
100
           * **********
110
            未未米+*********************
120
           130
           ************
140
           ***********
150
           ************
160
           **********
            (ADDRESS RZ) VCC =
       VS. TWP
                          5.00 V
          10
                30
                      50
                                  TAS
WPW
2.0
30
40
- 50
60
7υ
                   * *********
80
                 ********
90
100
         * 8**********
110
        **********
120
         *************
130
         ************
140
         *************
150
160
         ***********
```

```
VS. IMP (ADDRESS RZI) VCC = 10.0 V
   IAS
   -10
                                TAS
         10
               30
                     50
WPW
20
30
40
         ******************
50
         ************
60
         ******************
70
         **************
80
         ************
90
         ******************
100
         *****************
110
         *************
120
         ***********
130
         *************
140
         ************
150
         ***********
         *****************
160
   TAS V5. IMP
            (ADDRESS RZ)
                    VCC = 10.0 V
                                TAS
                     50
                           70
               30
WPW
20
30
40
         *******************
50
        *************
60
        ************
70
        **************
80
        90
        *************
        ****************
100
110
        *****************
120
        *************
        *******************
130
140
        *************
        ***********
150
        ********************
160
```

```
TAH
           VS. TWP
                   (ADDRESS RZI)
                                    VCC = 5.00 V
      -30
                -10
                           10
                                     TAH
wPw
 30
 40
 50
 60
                 * * * * *
 70
              **********
 80
               *********
 90
100
110
               *********
120
130
140
150
160
170
               *********
180
               *********
      HAI
           VS. TWP
                     (ADDRESS RZ)
                                    VCC = 5.00 V
      -30
                -10
                           10
                                     TAH
WPW
30
40
50
 60
 70
80
 90
100
110
120
130
140
150
160
170
                  ******
180
                  *******
```

.

) (†)

```
TAH
           VS. TWP
                      (ADDRESS RZI)
                                      VCC = 10.0 V
      -30
                            10
                                       TAH
wPw
 30
40
                     ******
50
60
70
80
90
100
110
120
130
140
150
                      *******
160
170
                      *****
180
                      *******
          VS. TWP
                      (ADDRESS RZ)
                                      VCC = 10.0 V
      ~30
                                       TAH
                            10
wPw
30
40
50
60
70
80
. 90
100
110
120
130
140
150
160
170
                        *****
180
```

```
TDS
         VS. TWP
                (DATA RZ1) VCC = 5.00 V
    - <u>i</u> ()
                             50
                                     TOS
             10
                     30
TWP
30
40
50
60
70
           ***********
80
            **************
90
            ***********
100
            **********
110
           **********
120
           *********
     TDS
         VS. TWP
                 (DATA RZ)
                          VCC =
                                5.00 V
    ~10
            1.0
                     30
                                    TDS
                             50
TWP
30
40
50
60
70
80
90
                   *******
100
                   *********
110
                   *********
120
                   **********
```

Ċ.

6.1

```
(DATA RZI) VCC = 10.0 \text{ V}
    TDS
       VS. TWP
                   30
                                 TDS
TWP
30
40
          ***********
50
60
          **********
70
          ************
03
          **********
90
          ************
100
          ***********
110
         **********
120
         *************
    TDS
       VS. TWP
               (DATA RZ) VCC =
                           10.0 V
                  30
           10
                          50
                                 TOS
TWP
30
40
            *************
50
            *************
60
             *************
70
             ************
80
            *********
90
            *************
100
            *********
110
           ********
120
```

40,5

```
(DATA RZI) VCC =
     HUI
            VS. TwP
                                          5.00 V
                           10
                -10
                                                 PDH
                                      30
TWP
30
 40
50
 60
 70
                       **********
80
 90
100
110
                      * * * * * * * * * * * * * * * * *
120
                      ******
      TOH
            VS. TWP
                      (DATA RZ) VCC =
                                          5.00 V
                           10
                                                TDH
                                      30
TwP
 30
 40
50
60
70
80
90
100
110
120
                            ********
```

C-25

.

```
HGT
         VS. TWP (DATA RZI) VCC = 10.0 V
                         30
             ≈10
                      10
                                      TOH
TWP
30
40
                   ********
50
                   **********
60
                    **********
70
                    *********
80
90
100
                    *********
110
                    **********
120
                    *********
         VS. TWP
                (DATA RZ) VCC = 10.0 V
                            30
     -30
                      10
             -10
                                      TDH
TWP
30
40
50
60
                      ******
70
                      ********
80
90
100
110
                      *****
120
                      ********
```

RCA CDP1822SD 256 X 4 CMOS STATIC RAM 08 MAY 79 TEMP: -55 C SN: 2

	ICC	٧s.	CACPE	TIN	åΕ		VCC	==	10.0V
	0		10	,	20			1	CC
CYCLE	•	•	-						
100.N						>			
200.N			د	ļ.		•			
400 . N			*						
800°N		*							
1.600		*							
3.20U		*							
6.40U	*								
12.80		*							
25.6U	*								
51.20		*							
102.U		*							
205.0	*								
410.U	*								
819.U	*								

DEVICE PASSED ALL TESTS

```
TAS
             (ADDRESS RZI)
                       VCC = 5.00 V
      VS. TWP
                                   TAS
         10
                30
                       50
                             70
wPw
20
30
40
50
60
                            ****
70
80
                       ******
                    ***********
90
100
                *************
             *********
110
          ************
120
130
          ***********
140
          ************
150
          *************
          *****************
160
      VS. TWP
             (ADDRESS RZ) VCC =
                          5.00 V
                       50
                                   TAS
          10
WPW
20
30
40
50
60
70
                      ********
80
                  ***********
90
100
            110
         ***********
120
       ****************
130
       *****************
140
       *************
150
       **********
160
```

TAH

TAH VS. TWP (ADDRESS RZI) VCC = 5.00 V

-30

180

-10

1

```
10
wPw
30
40
50
60
70
               ********
80
            **********
90
             *********
100
             **********
110
             **********
120
             *********
130
             ******
140
             **********
150
             *********
160
             **********
170
             ********
180
             *****
     PAH
         VS. IWF
                  (ADDRESS RZ)
                               VCC =
                                     5.00 V
                     10
     -30
             -10
                               TAH
WPW
30
40
50
60
70
              *********
80
               *******
90
100
110
120
130
```

```
rah
           VS. TWP
                      (ADDRESS RZI)
                                      VCC = 10.0 V
      -- 3 ()
                                      TAH
                -10
                            10
wPW
 30
 40
50
                   ******
 60
                   *******
 70
                    *******
 80
 90
100
110
120
                     *******
130
                     ******
140
150
160
170
                      ******
180
                      ******
      TAH
                      (ADDRESS RZ)
                                     VCC =
                                             10.0 V
           VS. TWP
      ~3()
                                      TAH
                            10
WPW
 30
 40
 50
 60
                      ******
 70
                       ****
 80
 90
100
110
120
130
140
150
160
170
180
                       ****
```

```
108
          VS. TWP (DATA RZI) VCC = 5.00 V
     -10
                         30
               10
                                  50
                                           TUS
TWP
30
40
50
60
10
80
                    *********
90
100
110
                   ***********
120
      rus
           VS. TWP
                    (DATA RZ) VCC = 5.00 V
                       30
                                  50
                                           TOS
TWP
30
40
50
60
70
80
90
100
110
                    ***********
120
                    **********
```

```
TOS VS. TWP
               (DATA RZI) VCC = 10.0 V
    -10 10
                   3 Q
                          50
                                  TOS
TwP
30
40
50
              ***********
60
              ************
70
              ***********
80
              ************
90
              ***********
100
             *******
110
             ***********
120
             ***********
        VS. TWP
                (DATA RZ) VCC = 10.0 \text{ V}
                         50
         10
                  30
                                 TDS
TWP
30
40
               **********
50
60
               ************
70
             ************
80
             ************
90
             *************
100
             ********
            **********
110
120
            ***********
```

-113

!---

```
TOH VS. TWP (DATA RZI) VCC = 5.00 V
                                              TDH
                -10
                           10
                                    30
Tw \vdash
 30
40
 50
 60
 70
 80
 90
100
110
120
                        ******
       for vs. Twe
                      (DATA RZ) VCC = 5.00 \text{ V}
                                   30
                0.1 **
                         10
      - 30
                                              TDH
TWF
30
4υ
50
60
70
80
90
100
110
120
```

```
VS. TWP
     TOH
                     (DATA RZI) VCC = 10.0 V
                                             TOH
     <del>-</del>30
               -10
                          10
                                   30
TWP
30
 4()
50
                        *********
60
70
80
                       ***********
90
                        *********
100
                        *********
110
                        *******
120
                        *******
      TOH
           VS. IMP
                     (DATA RZ)
                                VCC =
                                       10.0 V
                                             TOH
                          10
TWP
 30
 40
 5υ
                           *******
 60
 70
 80
 90
                            ******
100
                             ******
                             *****
110
                             ******
120
```

RCA CDP1822SD 256 X 4 CMOS STATIC RAM 08 MAY 79 TEMP: 125 C. SN:

ICC CYCLE TIME VS. VCC = 10.0V 10 20 ICC CYCLE 100.N 200.N 400.N 800.N 1,600 3.200 6.40U 12.80 25,60 51,20 102.U 205.U 410.U 819.0

DEVICE PASSED ALL TESTS

```
1AS
       VS. TWP (ADDRESS KZI)
                         VCC = 5.00 V
                   30
                                        TAS
    -10
                          50
           ΙÚ
                                 70
WPW
20
30
40
50
60
                                ****
70
                         *********
8.0
                      * * * * * * * * * * * * * * * * * * *
90
                  **************
100
               ***************
110
             ****************
120
               *****************
130
               *****************
140
150
             ***********
160
             ***********
    TAS
       VS. TWP
              (ADDRESS RZ)
                         VCC =
                              5.00 V
    -10
            10
                   30
                          50
                                 70
                                        TAS
WPW
20
30
40
50
60
                           ******
70
                      **********
80
                   *************
90
               **********
100
            **********
110
           ************
120
           ***********
130
            *************
140
           *****************
150
           ************
160
           ***************
```

```
TAS VS. TWP (ADDRESS RZI) VCC = 10.0 V
                   50
            30
   -10
                               TAS
        10
WPW
20
30
40
           **********
50
         **********
60
         *****************
70
         **********
80
         *************
90
         **************
100
         **********
110
         ***********
120
         **************
130
         **************
140
         **************
150
         ***********
160
         **********
     VS. TWP (ADDRESS RZ) VCC = 10.0 V
   TAS
   -10
        10
                          70
                               TAS
              30
                    50
WPW
20
30
40
           *****************
50
        ****************
60
        *******************
70
        ************
80
        ***********
90
        *************
100
        ***********
110
        ************
120
        *************
130
        ***************
140
        **********
150
        *******************
160
        ****************
```

```
(ADDRESS RZI) VCC = 5.00 V
        VS. TWP
             -10
                     10
                              TAH
    -30
wPw
30
40
50
              ******
6Ú
           *********
70
80
            ******
            ******
90
            *********
100
110
120
            *********
130
            ********
140
            *******
            ******
150
            ********
160
170
            180
            ********
                 (ADDRESS RZ) VCC = 5.00 V
         VS. TWP
     TAH
             -10
     -30
                     10
                              TAH
WPW
 30
 40
 50
 60
             ******
 70
              *********
 80
              ********
90
               *******
               *******
100
110
120
130
140
150
               *******
160
               *******
170
               *******
               *******
180
```

_ 1

TAH

VCC = 10.0 V

TAH

C-40

TAH VS. TWP (ADDRESS RZI) VCC = 10.0 V

10

***** *****

10

VS. TWP (ADDRESS RZ)

wPw 30 40

120

130

140

150

160

170

180

WPW 30 40

50

60

160 170

180

50 प्रकार समान्य १५

TAH

```
vCC = 5.00 \text{ V}
                (DATA RZI)
    TDS
         VS. IWP
                                    TOS
                            50
                    30
TWP
30
40
50
           ************
60
           **********
70
           ***************
80
           *********
90
           *********
100
           110
           **************
120
                 (DATA RZ)
                          VCC =
                               5.00 V
     1:138
         VS. TWP
                                    TOS
                    30
                            50
             10
    -10
TWP
30
40
50
                 **********
60
                 ***********
70
                 ***********
80
90
100
                 **********
110
                 **********
120
```

i i

t....

|& | |X

```
FDS VS. TWF (DATA RZI) VCC = 10.0 V
                       50
               30
    -10
        10
                               TDS
TWP
30
40
          *************
50
          ************
60
          ************
70
          *************
80
          **************
90
          *************
100
          **********
110
          *********
120
          *************
       VS. TWP (DATA RZ) VCC = 10.0 V
    TOS
                       50
                  30
           10
                              TDS
TWP
. 30
40
            ************
50
            ************
           **********
60
70
           ************
80
           *************
90
           ************
100
             ***********
110
           **********
120
           **************
```

```
TDH
           VS. TWP
                     (DATA RZI)
                                  VCC =
                          10
                                    30
                                              TOH
     -30
               -10
TWP
30
40
50
60
                       **********
70
                     **********
80
90
100
110
120
                 *************
      HUI
           VS. TWP
                     (DATA RZ)
                                 VCC =
                                    30
     -30
                          10
                                              TDH
TWP
30
40
50
60
70
80
                          ******
90
100
110
                          ********
120
                          ********
```

REPRODUCIBILITY OF THE ORIGINAL PACTOR POOR

4.17

```
TDH VS. TWP (DATA RZI) VCC = 10.0 V
    -30
                  10 30
            -10
                                     TDH
TWP
30
40
                  **********
50
                 **********
60
                  *********
70
                  ******
80
                  *********
90
                  **********
100
                  ********
110
                  **********
120
                  *********
     TDH VS, TWP (DATA RZ) VCC = 10.0 \text{ V}
                          30
    -30
                                     TOH
            -10
                     10
TWP
30
40
50
                     ********
60
                     ********
70
                     *******
80
90
100
110
                      ********
120
                      *******
```

RCA CDP1822SD 256 X 4 CMOS STATIC RAM 08 MAY 79 TEMP: 25 C. SW:

	TCC	VS.	CACPE	TlM	1£	AGC =	10.07
	o •	1	10	•	20	J	.cc
CACPE					· >		
100.N 200.N				*		٠	
400.H 800.N		*	, +				
1.60U 3.20U		* *					
6.400	*	*					
12.80 25.60	*	:					
51.20 102.0		* *					
205.U 410.U	‡ 1						
819.0	*						

DEVICE PASSED ALL TESTS

```
CDP1822SD 256 X 4 CMOS STATIC RAM 08 MAY 79
                                   TEMP: -55 C. SN:
    TAS VS. TWP (ADDRESS RZI) VCC = 5.00 V
    -10
           10
                  30
                        50
                                70
                                       TAS
WPW
20
30
40
50
60
                            * * * *
70
                       * ********
80
                   * ***********
90
                * *************
100
             * **************
110
            ************
120
            ***********
130
            *******************
140
            ***********
150
            ***********
160
            **********
    TAS VS. TWP (ADDRESS RZ) VCC = 5.00 V
    -10
           10
                  30
                        50
                                       TAS
wPw
20
30
40
50
60
                        * * * * * *
70
                   * * **********
80
                * **************
90
             * *****************
100
           * ******************
110
           ************
           ***********
120
130
           *************
140
           *************
150
           *************
160
           *********************
```

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```
(ADDRESS RZI) VCC = 10.0 V
   TAS VS. 1WP
   -10
              30
                                1 A S
                    50
                          7 Q
         10
WPW
20
30
40
          ***************************
50
         ************
60
         *********
79
         ************
80
         ************
90
         ************
         ***********
100
110
         *************
120
         ***********
130
         ********************
140
         ***************
15 U
         ************
160
         ***********
     VS. TWP (ADDRESS RZ)
                    VCC = 10.0 V
            30
        10
                    50
                               TAS
wPw
20
30
40
         **************
50
        ****************
60
        ********************
70
        ***********
        ***********
80
90
        ***************
100
        ************
        **********
110
          ***********
120
130
        *************
140
        ***************
        ***********
150
160
        *****************
```

1

(4)

```
TAH
        VS. TWP (ADDRESS RZI) VCC = 5.00 V
     -30
                              ľAH
             -10
                      10
wPw
30
40
50
60
                * * * * *
70
           **********
80
           *******
90
            **********
100
            ****
110
            *********
            ********
120
130
            ********
140
            ******
150
            *********
160
            **********
            ********
170 -
            *******
180
        VS. TWP (ADDRESS RZ) VCC = 5,00 V
     TAH
                              TAH
                      10
wPw
30
40
50
60
70
              ********
80
90
              *******
100
              ******
110
              *******
              ******
120
130
               ******
               ******
140
              *******
150
160
              *********
              ******
170
180
              *******
```

	ГАн	٧S.	TwP	(ADDRESS	RZI)	VCC =	10.0 V
	-30		-10	10		TAH	
wew							
30							
40				******			
50				******			
60				******			
70				*******			
8 o				*******			
90				******			
100				*****			
110				******			
120				******			
130				******			
140				******			
150				*****			
160				*****			•
170				*****			
180				*****			
100				******			
				•			
						į.	
	14H	٧S.	Twp	(ADDRESS	8Z)	VCC =	10.0 V
	-30		-10	10		TAH	
	1		1	1 1			
wPw							
30				•			
40				******			
50				****			
60				*****			
70				*****			
80				******			
90				*****			• .
100				******			
110				*****			
120				*****			
130	•			*****	•		
140				*****			
150				*****			
160				*****			
170				*****		٠ .	•
180				*****			
100				ուհ. ահ. ան. ան. ան. ակ.			

```
RCA CDP1822SD 256 X 4 CMOS STATIC RAM 08 MAY 79 TEMP: -55 C SN:
```

120

<u>}</u>

```
TDS
         VS. TWP
                 (DATA RZI) VCC = 5.00 V
                     30
     -10
             10
                                     TUS
                             50
TWP
30
40
50
60
70
            ************
80
            *************
90
            *************
100
            **********
110
            **********
120
            **********
     TDS
         VS. TWP
                (DATA RZ)
                         VCC = 5.00 V
     -10
             10
                     30
                             50
                                     TOS
TWP
30
40
50
60
70
80
90
100
110
                   *******
120
                   **********
```

```
TDS
        VS. TWP (DATA RZI) VCC = 10.0 V
    -10
           10
                   30
                          50
                                 TDS
TWP
30
40
          ************
50
          *************
60
          *************
70
          *************
80
          **************
90
          **************
100
          ************
110
          ************
120
          **********
    TOS VS. TWP (DATA RZ) VCC = 10.0 V
                        50
    -10
                30
           10
                                 TDS
                          1 .
TWP
30
40
            ************
50
            ********
60
            *************
70
           *************
80
           ************
90
           **************
100
           ************
110
           ************
120
            **************
```

```
RCA CDP1822SD 256 X 4 CMOS STATIC RAM 08 MAY 79 TEMP: -55 C SN:
```

```
HQI
          VS. TWP
                   (DATA RZI)
                              VCC = 5.00 V
     ~30
                                30
                                        1DH
TWP
 30
40
50
60
70
                   ***********
80
                 ***********
90
                ********
100
               ********
110
               *************
120
               ************
      TOH
          VS. TWP
                   (DATA R2)
                           vcc =
                                   5.00 V
                       10
                                30
                                        TDH
TWP
30
40
50
60
70
                       ********
80
                      *********
90
100
110
120
                      *********
```

```
TOH VS. TWP (DATA RZI) VCC = 10.0 V
              -10
                         10
     -30
                                            TDH
TwP
30
40
                     *********
50
                    ***********
60
                     ***********
70
                     * * * * * * * * * * * * * * *
80
90
100
110
                     *******
120
                     *********
      TOH
                    (DATA RZ) VCC = 10.0 V
           VS. TWP
                                 30
                        10
                                            TOH
     → 3 ()
               -10
TWP
 30
 40
                        *********
50
                        *********
 60
                        *********
 70
 80
 90
100
110
120
```

m ...

RCA CDP1822SD 256 X 4 CMOS STATIC RAM 08 MAY 79 TEMP: -55 C SN:

3

ICC VS. CYCLE TIME VCC = 10.0V 20 10 1CC CYCLE 100.N 200.N 400 N 800.N 1.600 3.20U 6.40U 12.80 25.6U 51.20 102.0 205.0 410.U 819.0

DEVICE PASSED ALL TESTS

1 4

1

. .

```
IAS
      VS. TWP (ADDRESS RZI) VCC = 5.00 V
   -10
          10
                       50
                                    TAS
wPw
20
30
40
50
60
70
80
                        *******
90
                     **********
100
                 *******
110
              **************
120
           *****************
130
          ************
140
          ***********
150
          ************
160
          **********
      VS. TWP (ADDRESS RZ) VCC = 5.00 V
   TAS
          10
                 30
                       50
                                    TAS
wPw
20
30
40
50
69
70
                          ******
80
                     *********
90
                  *************
100
               ***************
110
            ***********
120
        ************
130
          140
150
        *************
        **************
160
```

3

11

1

```
VS. TWP
                      VCC = 10.0 V
            (ADDRESS RZ1)
   TAS
          10
                            70
                                  TAS
WPW
20
30
                 ***********
40
             ************
50
          ************
60
70
         ************
80
          ******************
          ***********
90
100
          ************
         *************
110
120
          **********************
          *************
130
          ************
140
150
          *************
160
          ************
                      VCC =
      VS. TWP
             (ADDRESS RZ)
                          10.0 V
   -10
          10
                30
                      50
                            70
                                   TAS
WPW
20
30
                 *********
40
50
             ***************
         ************
60
        ************
70
        *************
80
        ***********************
90
        **************
100
110
120
        *********************
130
        ********************
140
        ***************
        ************
150
        **********************
160
```

```
(ADDRESS RZI)
                               VCC = 5.00 V
         VS. TwP
              -10
                                TAH
                       10
wPw
30
40
50
ь0
                *****
70
80
            **********
90
            **********
100
             *******
110
             *********
120
             *********
130
             *********
140
             ******
150
             *********
160
             **********
170
             ********
             **********
180
                               VCC = 5.00 V
     TAH
         VS. TWP
                  (ADDRESS RZ)
                                TAH
     -30
              -10
                        10
wPw
30
40
50
 60
 70
             **********
 80
              *******
90
               *********
100
                ******
110
                ********
120
                ********
130
                *******
140
                ********
150
160
170
180
                *******
```

```
TAH
          VS. TWP
                     (ADDRESS RZI)
                                    VCC =
                                           10.0 V
      -30
                -10
                          10
                                    TAH
wPw
 30
 40
                    *****
 50
                   *******
 60
                   *******
 70
                   ******
 80
                   *******
90
                   ******
100
                   *******
110
                    ******
120
                    ******
130
                    *******
140
                    ******
150
                    ******
160
170
                   *****
180
                    ******
          VS. TWP
     TAH
                    (ADDRESS RZ)
                                   VCC =
                                          10.0 V
     -30
                          10
                                    TAH
wPw
30
40
                  ******
50
                   ******
60
                    *****
70
                    ******
80
                    ******
90
                     ******
100
                     *****
110
                     ******
120
130
140
```

RCA CDP1822SD 256 X 4 CMOS STATIC RAM 08 MAY 79 TEMP: 125 C. SN:

```
-1DS VS. TWP (DATA RZI) VCC = 5.00 \text{ V}
                         50
    -10
         10
                30
                                  108
TWP
30
40
50
60
70
80
                 *****
90
                 **********
100
                **********
110
                **********
120
                **********
     rus
         VS. TWP
               (DATA RZ) VCC = 5.00 V
                30 50
           10
                                  TDS
TWP
30
40
50
60
70
80
                   *********
90
                 *****
100
110
                 ******
120
                *******
```

```
VS. TWP
              (DATA RZ1) VCC = 10.0 V
         10
                   30
                                 TUS
                           50
TWP
30
40
50
               **********
60
               **********
70
                 **********
80
90
               ***********
100
               ***********
110
              120
              **********
               (DATA RZ) VCC = 10.0 V
        VS. TWP
                                  TUS
TWP
30
40
                 ***
50
              **********
60
             ************
70
             ***********
80
             ************
90
100
110
120
             ***********
```

```
TOH VS. IWP (DATA RZI) VCC = 5.00 V
                    10 30
              -10
                                          TDH
TWP
 30
 40
 50
 60
 70
 80
 90
100
110
120
                   *************
     for VS. TWP
                  (DATA RZ) VCC = 5.00 V
                               30
                       10
     -30
                                          TOH
TWP
 30
 40
 50
 60
 70
- 80
 90
100
110
120
```

3 😅

-

```
TDH VS. TWP
                 (DATA RZI) VCC = 10.0 V
    -30
             -10
                     10
                             30
                                     IDH
TWP
30
40
50
                   *********
60
                   *****
70
80
                  ******
90
                  ***********
100
                  *********
110
                  *****
120
                   *******
     TDH
         VS. TWP
                 (DATA RZ) VCC = 10.0 V
                          30
                     10
                                    TDH
TwP
30
40
50
                      ********
60
                      *******
70
80
                      ********
90
                       *******
100
110
120
                       ******
```

	1CC	٧S.	CACTE	TIM	E	VCC =	10.0V
	0	ı	10	1	20	1	cc
CYCGE 100.N 200.N 400.N			*	举	>		
800.N 1.60U 3.20U		* *					
6.400 12,80 25.60 51.20	*						
102.0 205.0 410.0 819.0	* * *						

DEVICE PASSED ALL TESTS

4.4

```
TAS
       VS. TWP
             (ADDRESS RZI) VCC = 5.00 V
    -10
                 30
                       50
                              70
                                    TAS
wPw
20
30
40
50
60
                        * *****
70
                     **********
80
90
                  *************
               ***************
100
            110
120
            ************
130
            ***********
140
            ***********
150
            ************
            ***********
160
    TAS
       VS. PWP
             (ADDRESS RZ)
                       VCC = 5.00 V
           10
                 30
                                    TAS
                        50
                              70
WPW
20
30
40
50
60
70
                     *********
80
                  ************
               *****************
90
           ***********
100
         **************
110
120
         *************
130
         ****************
         ****************
140
150
         ********************
160
         ************
```

```
VS. TWP
   TAS
           (ADDRESS RZ1)
                    VCC = 10.0 V
   -10
                    50
                               TAS
        10
              30
WPW
20
30
40
           ***********
50
         60
         ************
70
        ************
80
         ***************
90
         ************
100
         *************
110
        120
         ************
130
         *************
140
         ************
150
        ***************
160
         ****************
   TAS
     VS. INP
           (ADDRESS RZ)
                  VCC = 10.0 \text{ V}
                               TAS
WPW
20
30
40
           ***************
50
        60
        ***********
70
       ********************
80
        ************************
90
        ***********
100
        ****************
110
       ***********************
120
        *****************
130
        ***********
140
        ******************
150
       **************
160
```

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

1.00

事

T

```
VS. TWP
                  (ADDRESS RZI) VCC = 5.00 V
                   10
             -10
     -30
                               TAH
WPW
30
40
50
60
                * * * * *
70
             *********
80
             *********
90
             *****
             ******
100
110
             ******
120
             *********
130
             *******
140
             ********
150
             *********
             ********
160
             *******
170
             **********
180
                              VCC = 5.00 V
     TAH
         VS. TWP
                  (ADDRESS RZ)
                     10
             -10
                               TAH
WPW
30
40
50
60
70
80
90
100
110
               ******
120
               ********
130
140
150
160
               ******
170
               ********
               ********
180
```

```
LAH
           VS. TWP (ADDRESS RZI) VCC = 10.0 V
                     10
      -30
                                     TAH
                -10
wPw
 30
 40
                   *******
50
                    ******
 60
70
80
90
                    *****
100
                     ******
110
120
130
                     ******
140
                     ******
150
                     ******
160
                     ******
                     *****
170
180
                     *****
      PAH
           VS. TwP
                    (ADDRESS RZ) VCC = 10.0 V
                       10
      <del>-</del>30
                                     TAH
                -10
wPw
30
 40
                     ******
 50
 60
 70
 80
90
100
110
120
130
140
150
160
170
180
                      *****
```

```
TOS VS. TWP (DATA RZI) VCC = 5.00 V
          10
                     50
                30
                                TUS
TWP
30
40
50
60
70
          **********
80
          ***********
90
          *************
100
          **********
110
          *********
120
          ***********
    าบธ
        VS. TWP
               (DATA RZ) VCC = 5.00 V
            10
                   30
                         50
                                TDS
PwP
30
40
50
60
                 *********
70
                 ********
80
90
                 *********
100
                 *********
110
                 **********
120
                 *********
```

```
TOS
           PaP
                (DATA RZI)
                         VCC =
                              10.0 V
    -1 ∪
                   30
                                  TDS
                           50
TwP
30
40
           **********
50
           ***************
60
           **************
70
           ***************
80
           ************
90
           ****************
100
           **********
110
120
           ***************
                              10.0 V
     TOS
        vo. IwP
                (DATA RZ)
                       v¢c =
                                  TDS
    -1U
                           50
TWP
30
40
             ************
50
             ***********
60
             *************
70
            ************
80
            ***************
90
100
            *******
            110
120
```

```
TDH
          VS. TWP (DATA RZI) VCC = 5.00 V
     =30
             -10
                      10
                                      TOH
                              30
TWP
30
40
50
60
70
                  ************
80
                ************
90
               ************
100
              ***********
110
             *********
120
             *********
     TDH
         VS. TWP
                  (DATA RZ)
                          VCC = 5.00 V
     -30
             -10
                      10
                              30
                                     TDH
TWP
30
40
50
60
                         *** ****
70
                       ********
80
                      *******
90
100
110
                      ********
120
                      ******
```

```
TOH VS. IWP
                 (DATA RZI) VCC = 10.0 V
                    10
     -30
             -10
                              30
                                      TDH
TWP
. 30
40
                   *********
50
                  ***********
 60
                  ********
 70
                   **********
 80
                   **********
90
                   ********
100
                   ***********
110
                  **********
120
                  **********
     TOH VS. TWP
                 (DATA RZ) VCC = 10.0 \text{ V}
          -10
                            30
    -3()
                                     TOH
TWP
30
40
                     ********
50
                      ********
60
                      ********
70
                      ********
80
                      *****
90
100
                      ********
110
                      ******
120
                      *******
```

	TCC	VS.	CYCL	E TI	ME		VCC	=	10.01
	0	,	10	,	20		1CC		CC
CXCTF	•	•	•	•	,				
100.N						>			
200 ° N				*					
400.N			*						
800*N		*							
1.600		*							
3,200		*							
6,400	*								
12.80	*								
25.60	*								
51,20		*							
102.0	*								
205.U	#	-							
410.U	*								
819.0	*								

DEVICE PASSED ALL TESTS

```
TAS VS. TWP
            (ADDRESS RZI)
                     VCC = 5.00 V
         10
             30
   -10
                      50
                                  TAS
WPW
20
30
40
50
00
70
                 * ***********
80
90
              * ***********
100
           * **************
           ***********
110
120
           ******************
130
           ************
140
150
           ************
           ************
160
     VS. TWP (ADDRESS RZ) VCC = 5.00 V
   TAS
                    50
               30
                           70
         10
   -10
                                   TAS
wPW
20
30
40
50
60
                 * * **********
70
              * ************
80
90
           * * **************
100
          ***************
         **********
110
120
         ******************
         ************
130
140
         ************
150
         *************
160
```

6.3

-

-

WPW 20 30 40 *********** 50 ************* 60 70 ************* 80 *********** 90 ************* 100 ************ 110 ***************** 120 ********** 130 ************* 140 ****************** 150 *********** 160 ***********

TAS VS. TWP (ADDRESS RZ) VCC = 10.0 V

```
(ADDRESS RZI) VCC = 5.00 V
     TAH VS. TWP
     -30
                      10
                                TAH
             -- 1 i)
w9w
30
40
50
60
70
            *********
80
            **********
90
            *******
100
            **********
110
            *********
120
            *********
130
            ********
140
            ***********
150
             **********
160
             ********
170
             *********
             *********
180
        VS. TwP
                               VCC = 5.00 V
     TAH
                  (ADDRESS RZ)
                      10
                                TAH
     -30
             -10
wPw
30
40
50
60
              * * * * * *
70
80
90
               ********
100
               ********
110
              *********
120
130
140
              ********
150
              ******
160
              ********
170
              *******
180
              *******
```

1.1.3

```
TAH
           VS. TWP
                    (ADDRESS RZI)
                                    VCC = 10.0 V
      -30
                      10
                -10
                                    TAH
WPW
 30
 40
                    *******
 50
                    ******
 60
                     ******
 70
                     ******
 80
                     ******
 90
                     *******
100
                     *****
110
                     *****
120
                     ******
130
                     ******
140
1.50
160
170
                     *******
180
                     *****
      TAH
           VS. TWP
                     (ADDRESS RZ)
                                  VCC =
                                         10.0 V
                      10
               -10
      --30
                                    TAH
WPW
 30
 40
 50
 60
 70
 80
 90
100
                      *****
110
                      *****
120
130
140
150
                      *****
160
170
                      *****
180
                      *****
```

```
TOS VS. TWP (DATA RZI) VCC = 5.00 V
          10
                   30
    -10
                              50
                                       TUS
TWP
30
40
50
60
70
             ************
80
             ********
90
100
             *************
110
             ************
120
            *************
     TDS
         VS. TWP
                  (DATA RZ) VCC = 5.00 \text{ V}
                      30
                                       TDS
     -10
              10
                              50
TWP
30
40
50
60
70
80
90
100
110
120
                      ********
```

i i

```
IDS VS. TWP (DATA RZI) VCC = 10.0 V
                    50
   -10 10
              30
                            TDS
IWP
30
         **********
40
50
         **********
60
         ********
70
         **********
80
         *********
90
         **********
100
         **************
110
        **************
        *********
120
    TOS VS. TWP (DATA RZ) VCC = 10.0 V
              30
                30 50
                           TDS
          10
TWP
30
            ***** * * * *
40
           **********
50
           ********
          ************
60
70
          *********
80
          ************
90
          *********
100
          ************
110
          ************
120
          ************
```

```
VS. TWP
                (DATA RZI) VCC = 5.00 V
                   10
                              30
                                       TDH
             <del>-</del>10
TWP
30
40
50
60
70
80
90
               **********
100
             *******
110
             ************
             ************
120
     TOH
         VS. TWP
                 (DATA RZ) VCC = 5.00 V
                      10
                              30
                                       TDH
TWP
30
40
50
60
70
                       *******
80
                     ********
90
                     *******
100
                       ********
110
                     *********
                     *********
120
```

t : .

```
TOH
        VS. TWP
                (DATA RZI) VCC = 10.0 V
                          -30
            -10
                     10
                                    TDH
IwP
30
40
                 ***********
50
                 **********
60
                 ***********
70
                  ***********
80
                  ******
90
                  **********
100
                  ******
110
                  *****
120
                  **********
     TDH
        VS. TWP
                 (DATA RZ) VCC = 10.0 V
            -10
                    10
                                    TDH
                            30
TWP
30
40
                    ********
50
60
                    ********
70
                    *********
80
                     *******
90
100
110
120
                    *****
```

RCA CDP1822SD 256 X 4 CMOS STATIC RAM 08 MAY 79 TEMP: -55 C SN: 4

10.0V ICC VS. CYCLE TIME VCC = 10 20 ICC CYCLE 100.N 200,N 400.N 800.N 1,600 3.200 6.400 12.80 25.60 51,20 102.0 205.U 410.U 819.0

DEVICE PASSED ALL TESTS

1.2

 $\bigcup_{i=1}^{n-1} \frac{\partial}{\partial x_i}$

```
VS. TWP
              (ADDRESS RZI)
                        VCC = 5.00 V
   TAS
                               70
                                      TAS
   -10
                  30
                        50
WPW
20
30
40
50
60
70
80
                          ******
90
                       *********
                   ********
100
110
             **********
120
130
           ************
           **************
140
          **************
150
          *****************
160
       VS. TWP
              (ADDRESS RZ)
                        VCC = 5.00 V
   TAS
                                      TAS
    -10
                        50
                               70
WPW
20
30
40
50
60
70
                         ********
80
                    ***********
90
                 ***********
100
              ************
110
          ************
120
        ************
130
        *************
140
        ***********
150
160
        *********************
```

```
VS. TWP
              (ADDRESS RZI)
                        VCC = 10.0 V
                         50
    ∞10
           10
                  30
                               70
                                      TAS
WPW
 20
 30
 40
                  *************
 50
              ******************
 60
            ******************
 70
           ********************
 80
            ******************
 90
           *****************
100
           ************
110
           ***********
120
           *******************
130
140
           ***************
150
           *************
160
           *************
              (ADDRESS RZ) VCC = 10.0 V
       VS. IWP
           10
                                      TAS
WPW
 20
 30
 40
                  **********
 50
             ************
 60
          *********************
 70
 80
           *****************
 90
         **********************
100
         **********************
110
         *********************
120
         ***************
130
         ******************
140
         ********************
150
         **************
1.60
         *****************
```

```
TAH VS. TWP (ADDRESS RZI)
                               VCC = 5.00 V
              -10
     -30
                                TAH
                      10
WPW
30
40
5ú
60
70
80
             **********
            **********
90
100
             *******
             ********
110
120
             *********
130
             *****
140
             **********
150
160
170
             *********
             ******
180
        vs. TWP (ADDRESS RZ)
                              VCC = 5.00 V
                     10
                                TAH
     -30
              -10
WPW
30
40
50
60
70
              *********
80
90
100
110
120
130
140
150
160
                *******
170
                ******
180
```

```
TAH
           VS. TWP
                    (ADDRESS RZI) VCC = 10.0 V
                      10
      -30
               -10
                                   TAH
wPw
 30
 40
                   ******
 50
                  *******
 60
 70
                  ******
 80
                   *******
 90
                   ******
100
110
120
130
140
150
                   ******
160
                   *******
170
                   ******
                   *****
180
                   (ADDRESS RZ) VCC = 10.0 \text{ V}
      TAH
           VS. TWP
      -30
                         10
                                   TAH
wPw
 30
 40
                  *******
 50
 60
 70
 80
                     *****
 90
                     *****
100
110
120
130
140
150
                     *****
160
                     ******
170
                     *****
180
                     *****
```

```
VS. TWP (DATA RZI) VCC = 5.00 V
     TDS
                         50
                     30
                                     TDS
TWP
30
40
50
60
70
80
90
100
                 ******
110
                 ************
120
                 ************
     108
         VS. TWP (DATA RZ) VCC = 5.00 V
             10
                          50
                  30
                                    TDS
TwP
30
40
50
60
70
80
90
100
110
                    ********
120
                   ******
```

```
1DS
         VS. TWP
                 (DATA RZI) VCC = 10.0 V
                                     TDS
             10
INP
30
40
50
               *************
               ***********
60
70
               ************
80
               ************
90
100
110
               ***********
120
         VS. TWP
                 (DATA RZ)
                          VCC =
                                    TOS
    -10
             10
                     30
                             50
TWP
30
40
                *********
50
60
              *************
70
              *************
80
              ************
90
              **********
100
               ************
              ***********
110
120
              *********
```

```
TDH VS. TWP (DATA RZI) VCC = 5.00 \text{ V}
                                 30
     <del>-</del>30
                          10
                                             TDH
TWP
30
40
50
60
70
80
                         *********
90
                       ******
100
110
                     *******
120
                    *******
      TOH VS. TWP (DATA RZ) VCC = 5.00 \text{ V}
               -10
      -30
                                    30
                                            TDH
                         10
TWP
30
40
50
60
70
80
90
100
110
120
```

```
TDH
           VS. TWP
                    (DATA RZI)
                                VCC = 10.0 V
                                           TDH
     -30
                         10
                                  30
TNP
 30
 40
50
                      **********
60
 70
80
90
100
                     ******
110
                     **********
120
      TOH
           VS. TWP
                    (DATA RZ)
                              VCC = 10.0 V
     -30
                         10
                                  30
                                           TDH
TWP
 30
 40
                          *******
 50
60
 70
                          ******
 80
90
100
                          ********
110
                          ********
120
                           ******
```

election of

RCA CDP1822SD 256 X 4 CMUS STATIC RAM 08 MAY 79 TEMP: 125 C. SN;

	TCC	٧S.	CYCLE	TIM	ΙE	VCC	=	10.0V
	O		10		20		ICC	
dvale.	ı	,	1	1	1			
CACPE								
100.N						>		
200.N				*				
400.N			*					
800.N		*						
1.600		*						
3.20U		*						
6.40U	*							
12.80		*						
25.6U	*							•
51.20		*						
102.U		*						
205.0	*							
410.0	*							
819.0	*							

DEVICE PASSED ALL TESTS